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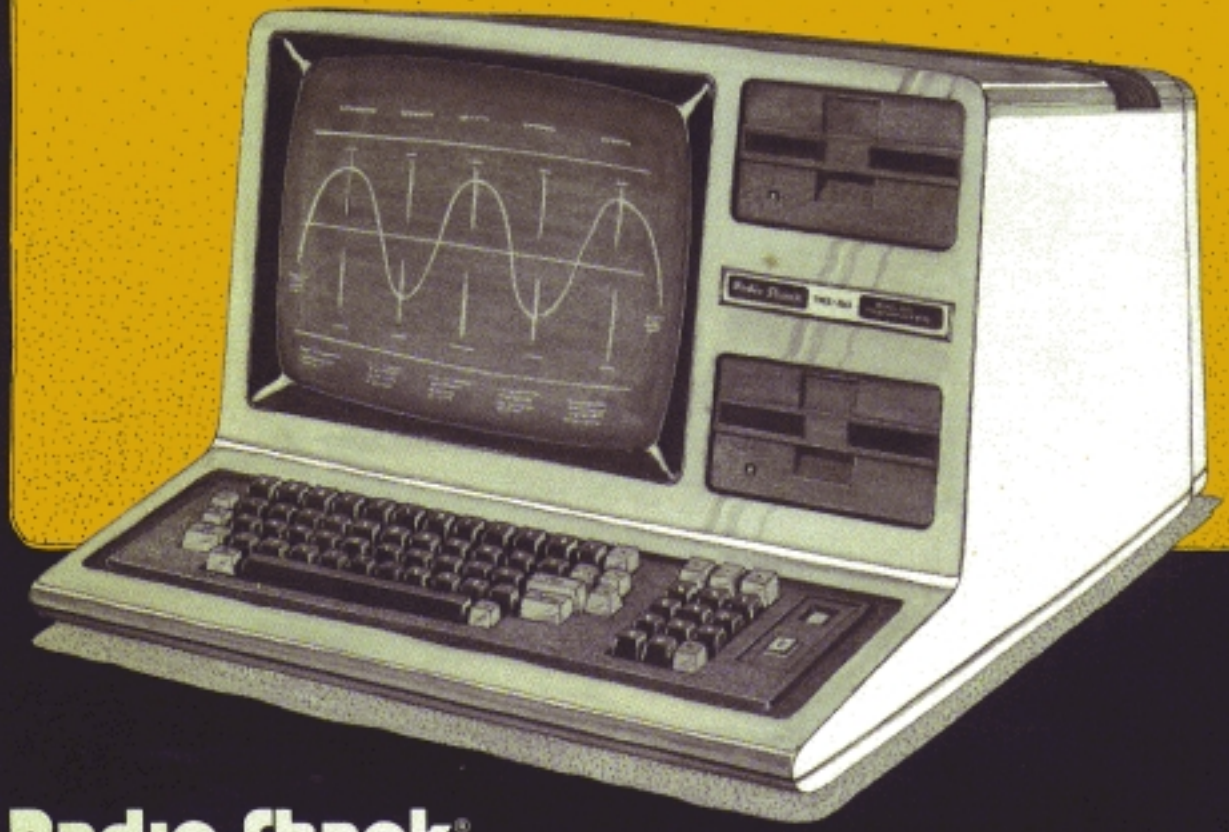
TRS-80® Model 4

Technical Reference Manual



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TRS-80®
MODEL 4
TECHNICAL
REFERENCE
MANUAL

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IMPORTANT NOTICE

This Technical Reference Manual is written for owners of the TRS-80 Model 4 Computer, who have a thorough understanding of electronics and computer circuitry. It is not written to the beginner's level of comprehension.

This manual contains detailed schematics and theories of operation for each major part of the Model 4. These tools will aid you with designing interfaces for your computer, repairing your own computer after its warranty has expired, or simply obtaining practical knowledge of your TRS-80 Model 4 operation.

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TABLE OF CONTENTS

Part 1 / Hardware

SECTION I **Introduction** **1**
1.1 SYSTEM OVERVIEW 3
1.2 BLOCK DIAGRAM 3
1.3 JUMPER OPTIONS 5

SECTION II **Disassembly / Assembly** **7**
2.1 Disassembly 9
2.1.1 Case 9
2.1.2 CPU Board 9
2.1.3 FDC Board (optional) 9
2.1.4 RS-232 Board (optional) 9
2.1.5 Main Power Supplies 9
2.1.6 Disk Drives (optional) 9
2.1.7 Video Monitor (CRT) and Video Board 10

2.2 Assembly 11
2.2.1 RS-232 Board (optional) 11
2.2.2 FDC Board (optional) 11
2.2.3 CPU Board 11
2.2.4 Power Supply 11
2.2.5 Disk Drive (optional) 11
2.2.6 Disk Drive Power Supply (optional) 11
2.2.7 Video Monitor (CRT) and Video Board 11
2.2.8 Case 11

SECTION III **CPU Circuit Board** **13**
3.1 Model 4 Theory of Operation 15
3.1.1 Introduction 15
3.1.2 CPU and Timing 15
3.1.3 Buffering 15
3.1.4 Address Decoding 15
3.1.5 ROM 19
3.1.6 RAM 19
3.1.7 Keyboard 19
3.1.8 Video 19
3.1.9 Real Time Clock 21
3.1.10 Cassette Circuitry 21
3.1.11 Printer Circuitry 21
3.1.12 I/O Connectors 21
3.1.13 Sound Option 21

3.2 Model 4 I/O Bus 26

3.3 Model 4 Port Bits 28

Schematic 8000173, 64K Version CPU PCB 8858090 31
CPU Component Layout 43
Parts List, CPU PCB #6700104AA3 45
Parts List, CPU PCB 8858090 49

SECTION IV **Floppy Disk Interface** **53**
4.1 Model 4 FDC PCB #8858060 55
4.1.1 Control and Data Buffering 55

4.1.2 Nonmaskable Interrupt Logic 55
4.1.3 Drive Select Latch and Motor On Logic 55
4.1.4 Wait State Generation and WAITIMOUT Logic 56
4.1.5 Clock Generation Logic 56
4.1.6 Disk Bus Selector Logic 56
4.1.7 Read/Write Data Pulse Shaping Logic 56
4.1.8 Disk Bus Output Drivers 56
4.1.9 Write Precompensation and Clock Recovery Logic 56
4.1.10 Floppy Disk Controller Chip 57
4.1.11 Adjustments and Jumper Options 57
FDC Board to CPU Board Signal Description 58
SCHEMATIC 8000095, PCB CONTROLLER #8858060 59
Parts List, FDC PCB #8858060 61

4.2 Model 4 FDC PCB #8858160 63
4.2.1 Control and Data Buffering 63
4.2.2 Nonmaskable Interrupt Logic 63
4.2.3 Drive Select Latch and Motor ON Logic 63
4.2.4 Wait State Generation and WAITIMOUT Logic 63
4.2.5 Clock Generation Logic 64
4.2.6 Disk Bus Selector Logic 64
4.2.7 Disk Bus Output Drivers 64
4.2.8 Write Precompensation and Write Data Pulse Shaping Logic 64
4.2.9 Clock and Read Data Recovery Logic 66
4.2.10 Floppy Disk Controller Chip 66
Schematic 8000268, FDC PCB #8858160 67
Component Layout, FDC PCB #8858160 69
Parts List, FDC PCB #8858160 71

SECTION V Mini-Disk Drive (not available) 73

SECTION VI Power Supplies (not available) 75

SECTION VII Video Monitor (not available) 77

SECTION VIII Exploded View / Parts List 79
Exploded View, Model 4 Computer, Catalog #26-1067/8/9 81
Parts List, Model 4 Computer, #26-1067/8/9 83

SECTION IX RS232C Circuit Board 85
9.1 RS-232C Technical Description 87
9.2 Pinout Listing 88
9.3 Port and Bit Assignments 89
RS-232 Board to CPU Board Signal Description 91
Schematic #8000076, RS232C Printed Circuit Board 93
Parts List, RS232C PC Board 95

LIST OF FIGURES

Fig. No.	Description	Page No.
1-1	TRS-80 Model 4 Interconnection Diagram	4
3-1	Model 4 Block Diagram	16
3-2	RAM Memory	20
3-3	Timing of U3 & CPU	23
3-4	Timing of U4	24
3-5	CPU Video Access Timing	25
3-6	I/O Bus Timing Diagram	27
4-1	Write Precompensation Timing	65

PART I
HARDWARE

SECTION I

INTRODUCTION

INTRODUCTION

1.1 SYSTEM OVERVIEW

The Radio Shack TRS-80 Model 4 Microcomputer is an enhanced version of Radio Shack's popular TRS-80 Model Ill Microcomputer. The TRS-80 Model 4 is software compatible with the Model Ill so that owners of either system can take advantage of the large number of programs available.

Features of the TRS-80 Model 4 which are common to the TRS-80 Model III include:

- Availability of Level I or Level II BASIC in ROM
- Full size typewriter style keyboard
- A 12-inch video display
- Built-in cassette interface
- Character display of 16 lines of 64 characters
- Graphics under control of BASIC (128 H x 48 V)
- UL recognized construction
- 12-key numeric keypad for rapid entry of numbers
- Rugged cabinet housing keyboard, electronics, video display, and power supply
- Direct drive video monitor for improved resolution
- Internal power supply
- Parallel printer port for use with Radio Shack printers

Other features available when Level II BASIC is used are: real time clock, upper and lower case characters, RAM internally expandable to 128K bytes, I/O port for peripheral expansion, and cassette interface available with 500 and 1500 baud rates.

Optional peripherals for the TRS-80 Model 4 include disk drives (two built-in, two external) with double density for increased storage capacity, and a built-in RS-232 serial interface for communications and peripheral interface.

1.2 BLOCK DIAGRAM

The Block Diagram (Figure 1-1) shows the various internal components and connections of the Model 4 Microcomputer.

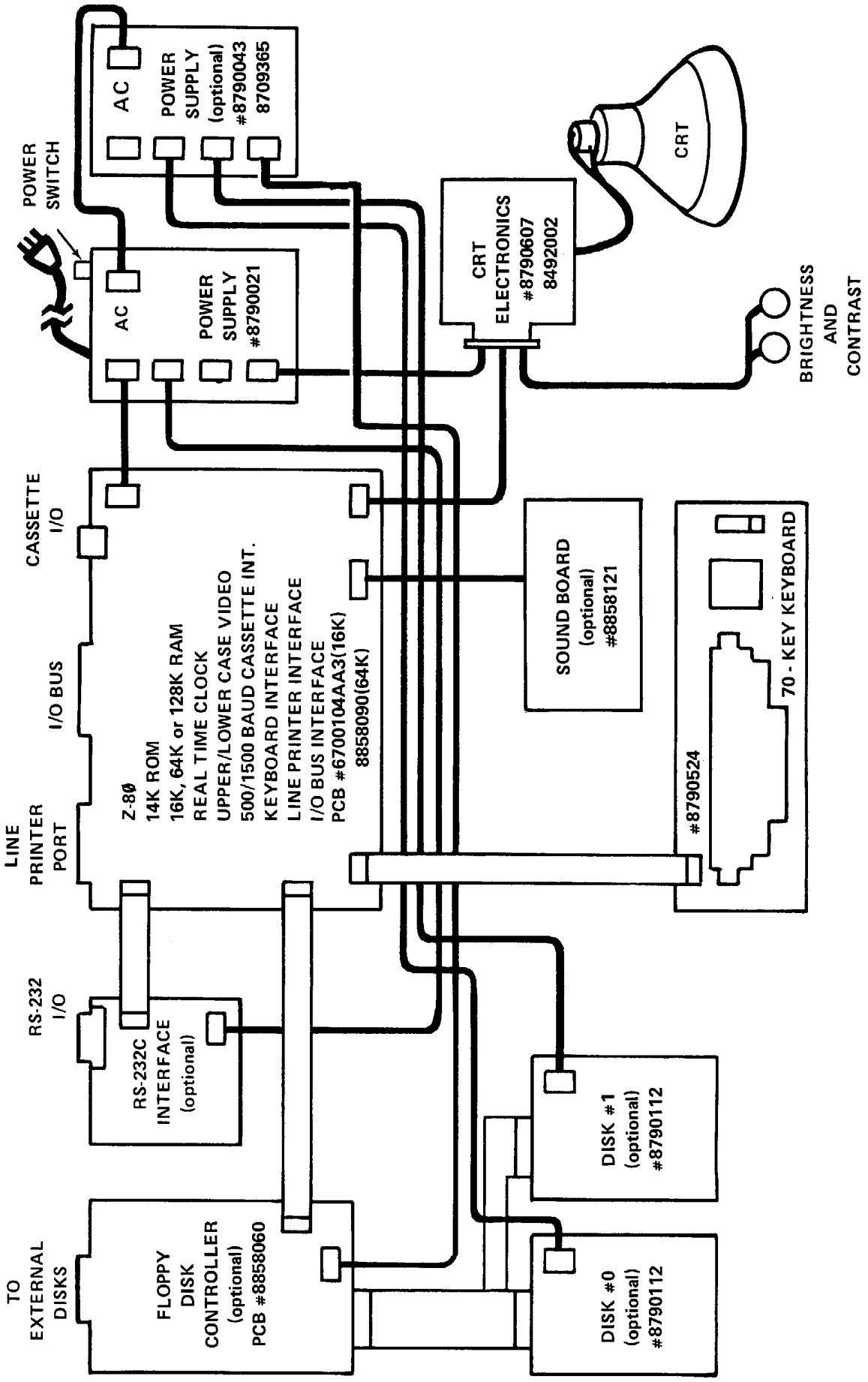


FIGURE 1-1. TRS-80 MODEL 4 INTERCONNECTION DIAGRAM

1.3 JUMPER OPTIONS

1.3.1 16K to 64K

1. Remove U77-U84
2. Move E5-E6 to E5-E4
   Move E1-E2 to E2-E3
   Move E12-E13 to E12-E11
3. Add E7-E8 and eight Tandy #8040665 ICs in locations U77-U84.
4. Remove capacitors 068, 072, 076, 080, 084, 088, 092 and 096.

1.3.2 64K to 128K

1. Remove shunt at U72 and add IC Tandy #8075468 in its place.
2. Add eight Tandy #8040665 ICs in locations U85-U92.

1.3.3 Graphics Board

1. Remove E14-E15 (and screws near U65 and U71).
2. Plug in Graphics Board
3. Replace mounting screws at U65 and U71.

1.3.4 E9-E10 are not used at this time

SECTION II

DISASSEMBLY / ASSEMBLY

DISASSEMBLY / ASSEMBLY

2.1 Disassembly

2.1.1 Case

1. Remove all cables from the bottom and rear of the Computer. Position the Computer on its rear panel to provide easy access to the case bottom. Remove the ten screws from the case bottom. Notice the different types and lengths of screws and note their positions. Set them aside in groups.
2. Position the Computer upright and remove the #6 screw and washer from the top of the back panel of the case.
3. Very carefully remove case top, lifting straight up and setting it aside to the left (if facing video screen). Be careful not to exceed the length of the video cable.
4. Remove screws from the chassis shield and the ground connectors and remove the shield.

2.1.2 CPU Board

1. Remove the six screws which attach the RFI Rear Shield to the metal CPU mounting bracket. This bracket is also held in place with tape at the lower part of the bracket. Carefully peel the tape away from the shield so that it may be reused.
2. Remove all cables connecting the CPU Board (power supply cable, video, keyboard, and cassette cables, and if applicable, the RS-232, sound board, and FDC interconnect cables).
3. Remove the eight screws fastening the CPU PCB (three at the top and bottom and one on either side of the board in the middle.
4. Make sure all cables to the CPU Board have been disconnected then remove the Board. (If your unit uses plastic spacer mounts to hold the Board, press the small tabs on the mounts through the mounting holes in the PCB and gently pull the CPU Board off.)

2.1.3 FDC Board (optional)

NOTE: The CPU Board must be removed before removing the FDC Board.

1. Be sure to disconnect all cables to the FDC Board.
2. Remove the screws holding the FDC Board to the metal chassis and remove the Board.

**Not applicable to all units.

2.1.4 RS-232 Board (optional)

NOTE: The CPU Board must be removed before removing the RS-232 Board.

1. Be sure to remove all cables connecting the RS-232 Board.
2. Remove the screws connecting the PC Board to the chassis and remove the Board.

2.1.5 Main Power Supplies

Three different power supplies are used on the Model 4 Computer, depending on the initial configuration of the unit. If the unit is supplied with 16K RAM and cassette input, Power Supply Assembly #879002 1 is supplied to provide DC voltages required to power the computer. It is mounted on the front side of the main CPU mounting bracket at the rear of the unit. If disk drive(s) are added to this computer, a second power supply is mounted to the LH disk drive mounting bracket.

If the computer is supplied with 64K RAM and a single or dual disk drive, then power supply #8790043 or #8790049 is supplied to power the unit. This power supply is mounted at the left side of the LH disk drive mounting bracket. It is attached to the CPU mounting bracket by screws through the heat sink bracket of the power supply.

1. Remove all interconnecting cables to the board(s). These include the power supply cable, video, keyboard, and cassette cable. If applicable, also remove the RS-232 and FDC power connectors and the disk ribbon cable.
2. Note the position of the ground tab and remove it.
3. Remove the screws which attach the power supply to its mounting support (four for the 38W power supply and two for the 65W power supplies). Spacers separate the 38W power supply from its mounting bracket. The 65W power supply is provided with insulated standoffs to prevent shorting the power supply against the metal disk drive shield bracket.
4. Carefully lift the power supply out of the computer. If the unit is one which has been upgraded to include a disk drive and is equipped with two power supplies, it may be necessary to remove the Main CPU mounting bracket to provide access to the mounting screws of one of the power supplies.

2.1.6 Disk Drives (optional)

1. To remove the Disk Drive in the top position, carefully remove the FDC inter-connect cable connected to the rear of the Drive. 2.

2. Remove the four screws and washers (two on each side) which connect the Drive to the Disk Mounting Bracket. Remove the RFI shield which covers the top drive.

3. Disconnect the power supply connector from the bottom of the top board in the Disk Drive and also remove the ground wire from the rear of the Drive.

4. To remove the Disk Drive in the bottom position, you must first remove the Power Supply attached to the LH Disk Mounting bracket to gain access to the Disk Drive mounting screws.

5. After removing the Power Supply, remove the FDC inter-connect cable from the rear of the Drive.

6. Remove the four screws and washers (two on each side) which connect the Drive to the Disk Mounting Bracket.

7. Disconnect the power supply connector from the bottom of the top board in the Disk Drive and also remove the ground wire from the rear of the Drive.

2.1.7 Video Monitor (CRT) and Video Board

1. Disconnect the four color coded wires with spade lugs from the CRT yoke. (Be sure to note their positions.)

2. Disconnect the connector on the rear of the CRT neck.

WARNING

There may be a high voltage charge on the high voltage anode. To discharge, connect one end of a wire to a known good ground and connect the other end of the wire to the blade of a common screwdriver. Insert the screwdriver blade under the suction cup and touch it to the clip holding the wire to the CRT.

Insert a common screwdriver under the suction cup on the high-voltage anode wire on the side of the CRT. Use the screwdriver to compress the clip holding the wire to the tube and pull the wire free.

3. Remove the ground wire fastened directly to the Video Board.

4. Remove the upper right and lower left nuts and washers which hold the CRT in place.

CAUTION

5. If dropped, the CRT may implode. To avoid this kind of accident, support the CRT while performing the next step.

6. Remove the remaining lower right and upper left nuts, and washers and carefully remove the CRT.

7. Disconnect the CPU cable connector from the Video Board.

8. Remove the two screws fastening the Video Board to the Case Top and carefully lift out Board.

2.2 Assembly

2.2.1 RS-232 Board (optional)

1. Install the PC Board using #6 x 1/4" screws. If applicable, press the PC Board onto the plastic spacer mounts then fasten with the screws.
2. Reconnect all cables to the RS-232 Board.

2.2.2 FDC Board (optional)

1. Install the PC Board using #6 x 1/4" screws and the plastic spacer mounts, if used.
2. Reconnect all cables to the FDC Board.

2.2.3 CPU Board

1. Make sure good insulating washers are attached to the CPU Board then fasten the Board using #6 x 1/2" screws,
2. Reconnect all cables to the CPU Board (power supply cable, video, keyboard, and cassette cables, and if applicable, RS-232 sound board, and FDC inter-connect cables),
3. Attach the small PCB Mount Bracket (if used) to the metal chassis bracket with two #6 x 1/4" screws.

2.2.4 Power Supply

1. Fasten the Power Supply to the CPU chassis bracket using #6 x 1/4" screws. Be sure the ground tab is fastened back in place.
2. Reconnect all cables (power supply, video, keyboard, and cassette cables, and RS-232 and FDC power cables and Disk ribbon cable if necessary).

2.2.5 Disk Drive (optional)

1. Place the Disk Drive in the bottom position and reconnect the ground wire and power supply connector.
2. Fasten the Drive with four #6-32 x 1/2" screws and four flat washers (two on each side).
3. Reconnect the FDC inter-connect cable to the rear of the Drive.
4. Position the second Disk Drive in the top position and reconnect the ground wire and power supply connector.
5. Fasten with four screws and washers (two on each side).
6. Reconnect the FDC inter-connect cable to the rear of the Drive.

2.2.6 Disk Drive Power Supply (optional)

1. Before installing the Power Supply be sure that the bottom Disk Drive is mounted in place and the Disk Shield is in position on the Disk Mounting Bracket.
2. Reconnect all cables and wires to the Power Supply.
3. Fasten the Power Supply with four #6 x 3/8" screws. Be sure the ground tab is fastened back in place.

2.2.7 Video Monitor (CRT) and Video Board

1. Position the CRT in the Case Top and install the upper left and lower right #10 washers and nuts.
2. Install the upper right and lower left #10 washers and nuts. Be sure to reconnect the ground wire from the CPU cable. It will require two nuts to fasten it.
3. Install the Video Board into the Case and fasten with two #6 x 3/8" screws.
4. Connect the ground wire with solder lug back to the Video Board.
5. Install the plug on the rear of the CRT neck.
6. Install the four color coded wires with spade lugs to their associated terminals (as determined by a colored dot on the yoke near each terminal).
7. Install the high-voltage anode wire on the side of the CRT. Use a screwdriver to compress the clip and insert it into the CRT. Press down on the suction cup to secure.

2.2.8 Case

1. 1, Double-check to be sure all wires are connected correctly and all Boards are properly fastened.
2. Attach the chassis shield (if used) with #6 x 1/4" screws and reconnect the ground connectors.
3. Carefully place the Case Top over the Case Bottom. Do not hit the CRT neck. It could implode or break off.
4. Install the #6 x 3/8" sheet metal screw and flat washer in the top rear panel of the Case.
5. Carefully rest the Computer on its rear panel and replace the ten #8 screws; five 1" sheet metal toward rear, three 7/8" machine head along front, and two 1" machine head in remaining positions.

SECTION III

CPU CIRCUIT BOARD

CPU CIRCUIT BOARD

3.1 Model 4 Theory of Operation

3.1.1 Introduction

The TRS-80 Model 4 Microcomputer is a self-contained desktop microcomputer designed not only to be completely software compatible with the TRS-80 Model Ill, but to provide many enhancements and features. System distinctions which enable the Model 4 to be Model Ill compatible include: a Z80 CPU capable of running at a 4 MHz clock rate, BASIC operating system in ROM (14K), memory-mapped keyboard, 64-character by 16-line memory-mapped video display, up to 128K Random Access Memory, cassette circuitry able to operate at 500 or 1500 baud, and the ability to accept a variety of options. These options include: one to four 5-1/4 inch double density floppy disk drives, one to four five megabyte hard disk drives, an RS-232 Serial Communications Interface, and a 640 by 240 pixel high resolution graphics board.

3.1.2 CPU and Timing

The central processing unit of the Model 4 microcomputer is the Z80-A microprocessor capable of running at either a two (2.02752) or four (4 .05504) MHz clock rate. The main CPU timing comes from the 20 MHz (20.2752 MHz) crystal-controlled oscillator, Y1 and 01. There is an additional 12 MHz (12.672 MHz) oscillator, Y2 and 02, which is necessary for the 80 by 24 mode of video operation. The oscillator outputs are sent to two Programmable Array Logic (PAL) circuits, U3 and U4, for frequency division and routing of appropriate timing signals.

PAL U3 divides the 20 MHz signal by five for 4 MHz CPU operation, by ten for a 2 MHz rate, and slows the 4 MHz clock for the Ml Cycle (See Figure 3-3). U3 also divides the master clock by four to obtain a 5 MHz clock to be sent to the RS-232 option connector as a reference for the baud rate generator. PAL U4 selects an appropriate 10 MHz or 12 MHz clock for the video shift clock, and using divider US provides additional timing signals to the video display circuitry (See Fig. 3-4).

Hex latch U18 is clocked from the 20 MHz clock, and is used to provide MUX and CAS timing for the dynamic memory circuits. Also, with additional gates from U16, U19, U20, U31, and U32, this chip provides the wait circuitry necessary to prevent the CPU from accessing video RAM during the active portion of the display. This is done by latching the data for the video RAM and simultaneously forcing the Z80 CPU into a “WAIT” state and is necessary to eliminate undesirable “hashing” of the video display (See Fig. 3-4).

3.1.3 Buffering

Low level signals from and to the CPU need to be buffered, or current amplified in order to drive many other circuits. The 16 address lines are buffered by U55 and U56, which are unidirectional buffers that are permanently enabled. The eight data lines are buffered by U71. Since data must flow both to and from the CPU, U71 is a bi-directional buffer which can go into a three-state condition when not in use. Both direction and enable controls come from the address decoding section.

The clock signal to the CPU (from PAL U3) is buffered by active pullup circuit 03 RESET and WAIT inputs to the CPU are buffered by U17 and U46. Control outputs from the Z80 (M1*, RD*, WR*, MREQ*, and IORQ*) are sent to PAL U58, which combines these into other appropriate control signals consistent with Model 4’s architecture. Other than MREQ*, which is buffered by part of U38, the raw control signals go to no other components, and hence require no additional buffering.

3.1.4 Address Decoding

The address decoding section is divided into two sub-sections: Port address decoding and Memory address decoding.

In port address decoding, low order address lines (some combined through a portion of U32) are sent to the address and enable inputs of U48, U49, and USO. U48 is also enabled by the IN~ signal, which means that is decodes port input signals, while U49 decodes port output signals. A table of the resulting port map is shown below:

	Port Addr. (Hex)	Read Function	Write Function
	FC - FF	Cassette In, Mode Read	Cassette Out, resets cassette data latch
	F8 - FB	Read Printer Status	Output to Printer
(1)	F4 - F7	-reserved-	Drive Select latch
(1)	F3	FDC Data Reg.	FDC Data Reg.
(1)	F2	FDC Sector Reg.	FDC Sector Reg.
(1)	F1	FDC Track Reg.	FDC Track Reg.

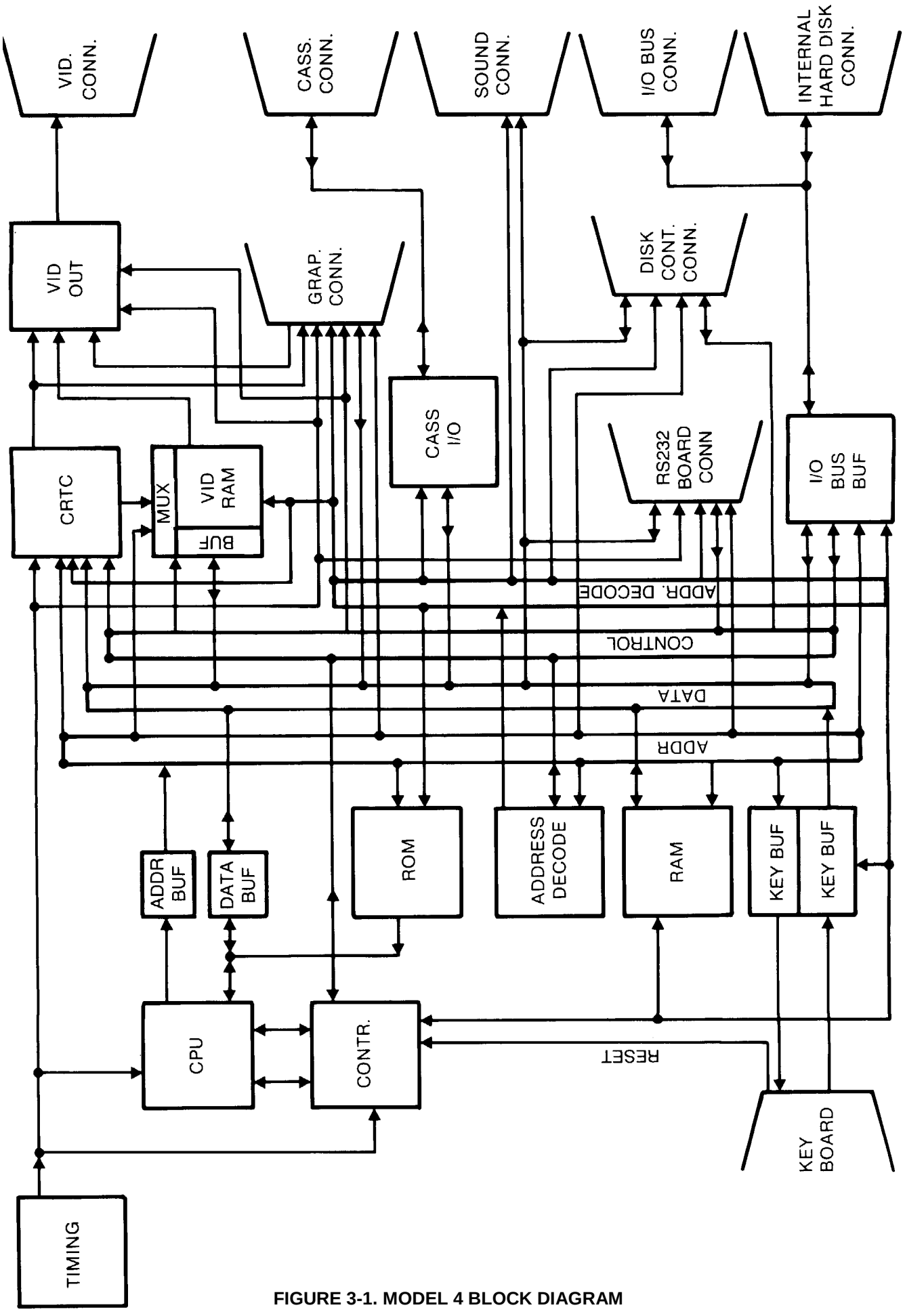


FIGURE 3-1. MODEL 4 BLOCK DIAGRAM

(1)	F0	FDC Status Reg.	FDC Command Reg.
	EC - EF	Resets RTC Int.	Mode Output latch
(2)	EB	Rcvr Holding Reg.	Xmit Holding Reg.
(2)	EA	UART Status Reg.	UART/Modem control
(2)	E9	-reserved-	Baud Rate Register
(2)	E8	Modem Status UART control reg.	Master Reset/Enable
	E4 - E7	Read NMI Status	Write NMI Mask reg.
	E0 - E3	Read INT Status	Write INT Mask reg.
(3)	CF	HD Status	HD Command
(3)	CE	HD Size/Drv/Hd	HD Size/Drv/Hd
(3)	CD	HD Cylinder high	HD Cylinder high
(3)	CC	HD Cylinder low	HD Cylinder low
(3)	CB	HD Sector Number	HD Sector Number
(3)	CA	HD Sector Count	HD Sector Count
(3)	C9	HD Error Reg.	HD Write Precomp.
(3)	C8	HD Data Reg.	HD Data Reg.
(3)	C7	HD CTC channel 3	HD CTC channel 3
(3)	C6	HD CTC channel 2	HD CTC channel 2
(3)	C5	HD CTC channel 1	HD CTC channel 1
(3)	C4	HD CTC channel 0	HD CTC channel 0
(3)	C2 - C3	HD Device 10 Reg.	- reserved -
(3)	C1	HD Control Reg.	HD Control Reg.
(3)	C0	HD Wr. Prot. Reg.	- reserved -
	94 - 9F	-reserved-	-reserved-
(4)	90 - 93	-reserved-	Sound Option
(5)	8C - 8F	Graphics Sel. 2	Graphics Sel. 2
	8B	CRTC Data Reg.	CRTC Data Reg.
	8A	CRTC Control Reg.	CRTC Control Reg.
	89	CRTC Data Reg.	CRTC Data Reg.
	88	CRTC Control Reg.	CRTC Control Reg.
	84 - 87	-reserved-	Options Register
(5)	83	-reserved-	Gra. X Rag. Write
(5)	82	-reserved-	Gra. Y Rag. Write
(5)	81	Graphics Ram Rd.	Graphics Ram Wr.
(5)	80	-reserved-	Gra. Options Reg. Wr

Notes: (1) Valid only if FOC option is installed
(2) Valid only if RS-232 option is installed
(3) Valid only if Hard Disk option is installed
(4) Valid only if sound option is installed
(5) Valid only if High Resolution Graphics option is installed

Following is a Bit Map of the appropriate ports in the Model 4. Note that this is an “internal” bit map only. For bit maps of the optional devices, refer to the appropriate section of the desired manual.

Model 4 Port Bit Map

Port	D7	D6	D5	D4	D3	D2	D1	D0
FC-FF	Cass							Cassette
(READ)	Data 500 bd			(MIRROR of PORT EC)				Data 1500 bd
FC - FF			(Note, also resets cassette data latch)				cass.	cassette
(WRITE)	x	x	x	x	x	x	out	data out
F8 - FB	Prntr	Prntr	Prntr	Prntr	x	x	x	x
(READ)	BUSY	Paper	Select	Fault	x	x	x	x
F8 - FB	Prntr	Prntr	Prntr	Prntr	Prntr	Prntr	Prntr	Prntr
(WRITE)	D7	D6	D5	D4	D3	D2	D1	D0
EC - EF			(Any Read causes reset of Real Time Clock Interrupt)					
EC - EF	x	CPU	x	Enable	Enable	Mode	Cass	x
(WRITE)	x	Fast	x	EX I/O	Altset	Select	Mot On	x
E0 - E3	x	Receive	Receive	Xmit	10 Bus	RTC	C Fall	C Rise
(READ)	x	Error	Data	Empty	Int	Int	Int	Int
E0 - E3	x	Enable	Enable	Enable	Enable	Enable	Enable	Enable
(WRITE)	x	Rec Err	Rec Data	Xmit Emp	10 Int	RT Int	CF Int	CR Int
90-93	x	x	x	x	x	x	x	Sound
(WRITE)	x	x	x	x	x	x	x	Bit
84 - 87	Page	Fix Upr	Memory	Memory	Invert	80/64	Select	Select
(WRITE)		Memory	Bit 1	Bit 0	Video		Bit 1	Bit 0

Memory mapping is accomplished by PAL U59 in the Basic 16K or 64K computer. In a 128K system, PAL U72, along with the select and memory bits of the options register, also enter into the memory mapping function.

Four memory maps are listed below. Memory Map I is compatible with the Model III. Note that there are two 32K banks in the 64K system, which can be interchanged with either position of the upper two banks of a 128K system. The 128K system has four moveable 32K banks. Also note, in the Model III mode, that decoding for the printer status read (37E8 and 37E9 hexadecimal) is accomplished by U93 and leftover gates from U40, U46, U51, U54, U60, and U62.

Memory Map I - Model III Mode

```
      0000 - 1FFF     ROM A (8K)
      2000 - 2FFF     ROM B (4K)
      3000 - 37FF     ROM C (2K) - Less 37E8 - 37E9
      37E8 - 37E9     Printer Status Port
      3800 - 38FF     Keyboard
      3C00 - 3FFF     Video RAM (Page bit selects 1K of 2K)
*     4000 - 7FFF     RAM (l6Ksystem)
*     4000 - FFFF     RAM (64K system)
```

Memory Map II

```
      0000 - 37FF     RAM (14K)
      3800 - 38FF     Keyboard
```

3C00 - 3FFF	Video RAM
4000 - 7FFF	RAM (16K) End of one 32K Bank
8000 - FFFF	RAM (32K) Second 32K Bank

Memory Map III

0000 - 7FFF	RAM (32K) End of One 32K Bank
8000 - F3FF	RAM (29K) Second 32K Bank
F400 - F7FF	Keyboard
F800 - FEFF	Video RAM

Memory Map IV

0000 - 7FFF	RAM (32K) One 32K Bank
8000 - FFFF	RAM (32K) Second 32K Bank

(See Figure 3-2 for 128K Maps)

3.1.5 ROM

The Model 4 Microcomputer contains 14K of Read Only Memory (ROM), which is divided into an 8K ROM (U68), a 4K ROM (U69), and a 2K ROM (U70). ROMs used have three-state outputs which are disabled if the ROMs are deselected. As a result, ROM data outputs are connected directly to the CPU data bus and do not use data buffer U71, which is disabled during a ROM access.

ROMs are Model III compatible and contain a BASIC operating system, as well as a floppy disk boot routine. The enable inputs to the ROMs are provided by the address decoding section, and are present only in the Model III mode of Operation.

3.1.6 RAM

Three configurations of Random Access Memory are available on the Model 4:16K, 64K, and 128K. The 16K option uses 4116 type, 16K by 1 dynamic RAMs, which require three supply voltages (+12 volts, +5 volts, and -5 volts). The 64K and 128K options use 6665 type, 64K by 1 dynamic RAMs, which require only a single supply voltage (+5 volts). The proper voltage for each option is provided by jumpers.

Dynamic RAMs require multiplexed incoming address lines. This is accomplished by ICs U63 and U76. Output data from RAMs is buffered by U64. With the 128K option, there are two rows of the 64K by 1 RAM ICs. The proper row is selected by the CAS signal from PAL U72.

3.1.7 Keyboard

The Model 4 Keyboard is a 70-key sculptured keyboard, scanned by the microprocessor. Each key is identified by its column and row position. Columns are defined by address lines AO - A7, which are buffered by open-collector drivers U29 and U30. Data lines DO - D7 define the rows and are buffered by CMOS buffers U44 and U45. Row inputs to the buffers are pulled up by resistor pack RP 1, unless a key in the current column being scanned is depressed. Then, the row for that key goes low.

3.1.8 Video

The heart of the video display circuitry in the Model 4 is the 68045 Cathode Ray Tube Controller. The CRTC allows two screen formats: 64 by 16 and 80 by 24. Since the 80 by 24 screen requires 1,920 screen memory locations, a 2K by 8 static RAM is used for the Video RAM. The 64 by 16 mode has a two-page screen display and a bit in the options register for determining which page is active for the CPU. Offset the start address of the CRTC to gain access to the second page in the 64 by 16 mode.

Addresses to the video RAM are provided by the 68045 when refreshing the screen and by the CPU when updating the data. These two sets of addresses are multiplexed by U33, U34, and U35. Data between the CPU and Video RAM is latched by U6 for a write, and buffered by U7 for a read operation.

During screen refresh, the data outputs of the Video RAM (ASCII character codes) are latched by U8 and become the addresses for the character generator ROM (U23). In cases of low resolution graphics, a dual 1 of 4 data selector (U9) is the cell generator, with additional buffering from U10

The shift register U1 inputs are the latched data outputs of the character or cell generator. The shift clock input comes from the PAL U4, and is 10.1376 MHz for the 64 by 16 mode and 12.672 MHz for 80 by 24 operation. The serial output from the shift register later becomes actual video dot information.

Special timing in the video circuit is handled by hex latch U2. This includes blanking (originating from CRTC) and shift register loading (originating from U4). Additional video control and timing functions, such as sync buffering, inversion selection, dot clock chopping, and graphics disable of normal video, are handled by miscellaneous gates in U12, U13, U14, U22, U24, and U26.

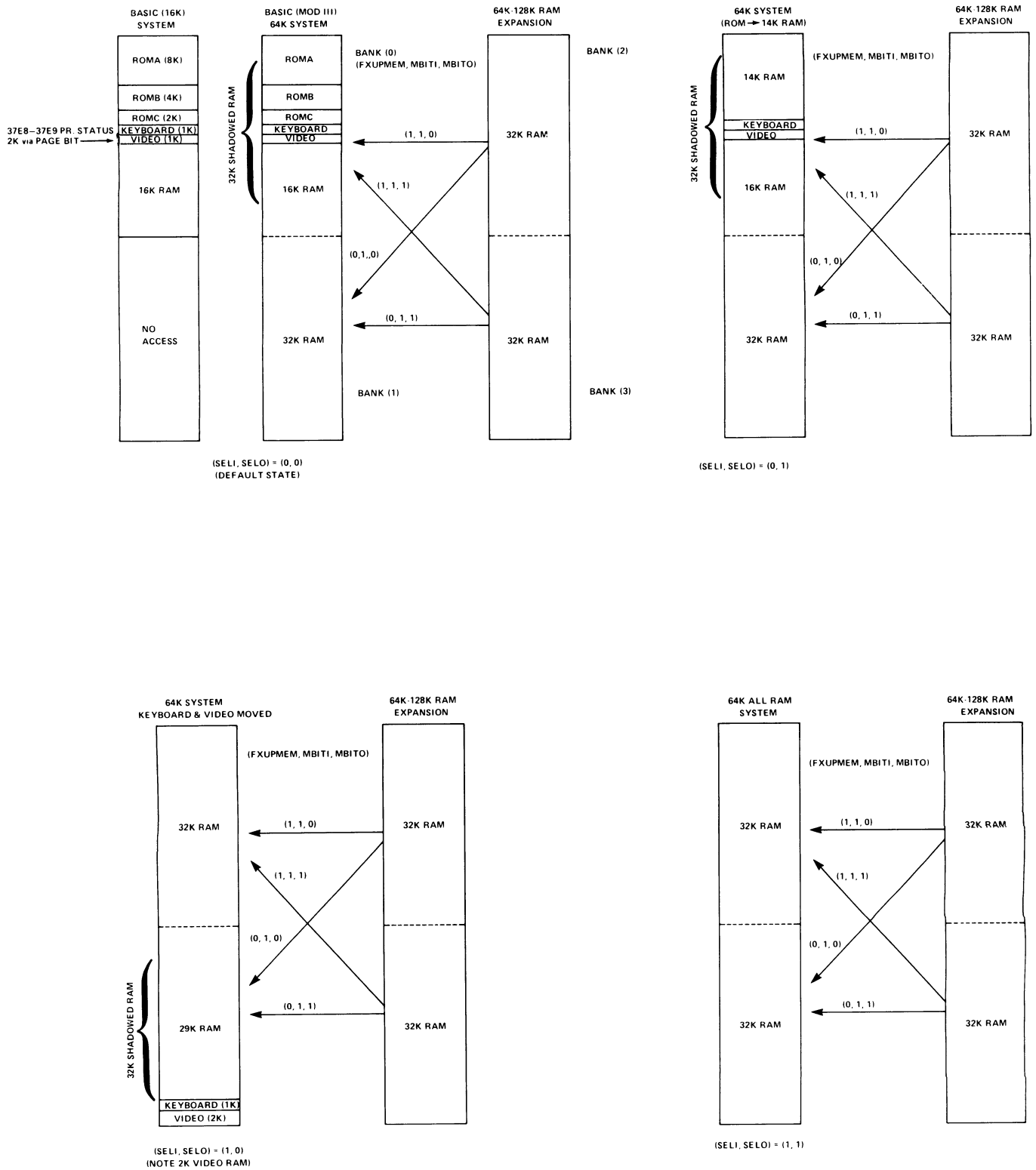


FIGURE 3-2. RAM MEMORY

3.1.9 Real Time Clock

The Real Time Clock circuit in the Model 4 provides a 30 Hz (in the 2 MHz CPU Mode) or 60 Hz (in the 4 MHz CPU Mode) interrupt to the CPU. By counting the number of interrupts that have occured, the CPU can keep track of the time. The 60 Hz vertical sync signal from the video circuitry is divided by two (2 MHz Mode) by U53, and the 30 Hz at pin 1 of U51 is used to generate the interrupts. In the 4 MHz mode, signal FAST places a logic low at pin 1 of U51, causing signal VSYNC to trigger the interrupts at the 60 Hz rate. Note that any time interrupts are disabled, the accuracy of the clock suffers.

3.1.10 Cassette Circuitry

The cassette write circuitry latches the two LSBs (DO and Dl) for any output to port FE (hex). The outputs of these latches (U27) are then resistor summed to provide three discrete voltage levels (500 Baud only). The firmware toggles the bits to provide an output signal of the desired frequency at the summing node.

There are two types of cassette Read circuits - 500 baud and 1 500 baud. The 500 baud circuit is compatible with both Model 1 and III The input signal is amplified and filtered by Op amps (U43 and U28. Part of U15 then forms a Zero Crossing Detector, the output of which sets the latch U40. A read of Port FF enables buffer U41, which allows the CPU to determine whether the latch has been set, and simultaneously resets the latch. The firmware determines by the timing between settings of the latch whether a logic one or "zero" was read in from the tape.

The 1500 baud cassette read circuit is compatible with the Model III cassette system. The incoming signal is compared to a threshold by part of U15. U15's output will then be either high or low and clock about one-half of U39, depending on whether it is a rising edge or a falling edge, If interrupts are enabled, the setting of either latch will generate an interrupt. As in the 500 baud circuit, the firmware decodes the interrupts into the appropriate data.

For any cassette read or write operation, the cassette relay must be closed in order to start the motor of the cassette deck. A write to port EC hex with bit one set will set latch U42, which turns on transistor Q4 and energizes the relay K1. A subsequent write to this port with bit one clear will clear the latch and de-energize the relay.

3.1.11 Printer Circuitry

The printer status lines are read by the CPU by enabling buffer U67. This buffer will be enabled for any input from port F8 or F9, or any memory read from location 37E8 or 37E9 when in the Model III mode. For a listing of bit status, refer to the bit map.

After the printer driver software determines that the printer is ready to receive another character (by reading the status), the character to be printed is output to port F8. This latches the character into U66, and simultaneously fires the one-shot U65 to provide the appropriate strobe to the printer.

3.1.12 I/O Connectors

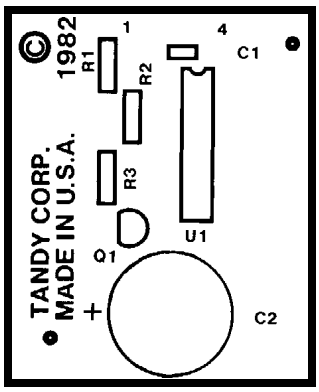
Two 20-pin single inline connectors, J7 and J8, are provided for the connection of a Floppy Disk Controller and an RS-232 Communications Interface, respectively. All eight data lines and the two least significant address lines are routed to these connectors. In addition, connections are provided for device or board selection, interrupt enable, interrupt status read, interrupt acknowledge, RESET, and the CPU WAIT signal.

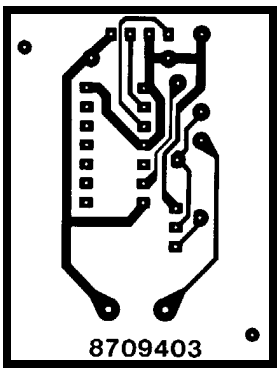
The graphics connector, J10, contains all of the above interface signals, plus CRTCLK, the dotclock signal, a graphics enable input, and other timing clocks which synchronize the graphics board with the CRTC.

The I/O bus connector, J2, contains connections for all eight data lines (buffered by U74), the low order address lines (buffered by U73), and the control lines (buffered by U75) IN*, OUT*, RESET*, M1*, and IORQ*. In addition, the I/O bus connector has inputs to allow the device(s), connected to generate CPU WAIT states and interrupts. The sound connector, J11, contains only four connections: sound enable (any output to port 90 hex), data bit D0, Vcc, and ground.

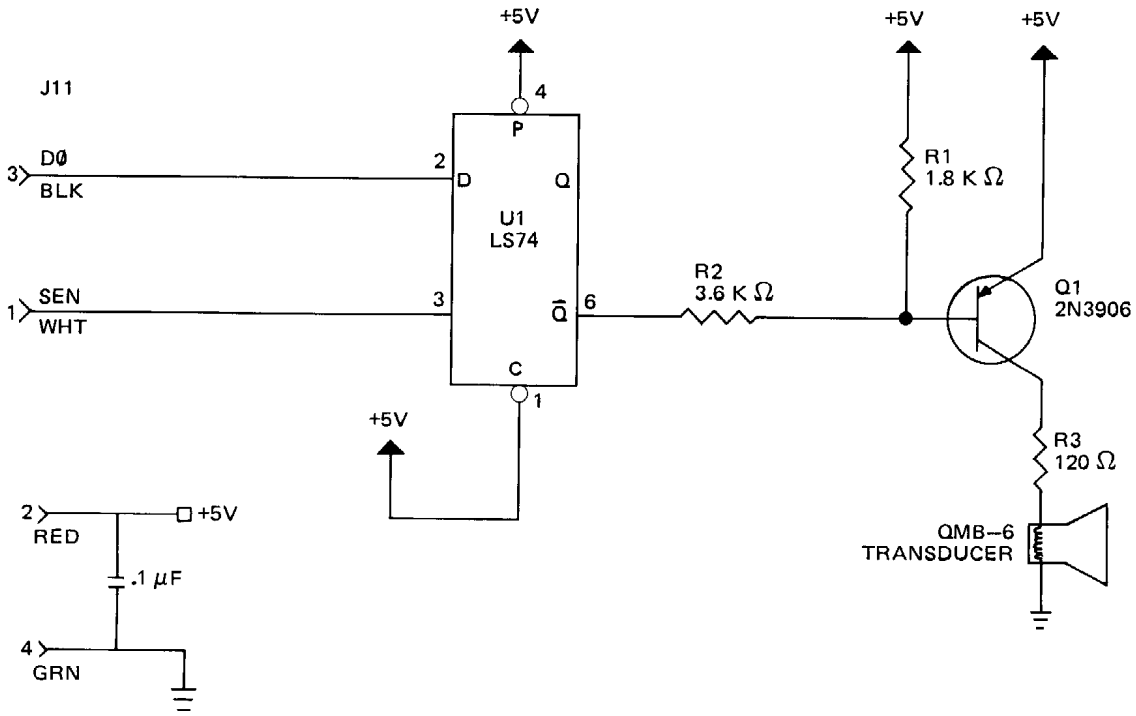
3.1.13 Sound Option

The Model 4 sound option, available as standard equipment on the disk drive versions, is a software intensive device. Data is sent out to port 90H, alternately setting and clearing data bit D0. The state of this bit is latched by sound board U1 and amplified by sound board Q1, which drives a piezoelectric sound transducer. The speed of the software loop determines the frequency, and thus, the pitch of the resulting tone.





COMPONENT LOCATION / CIRCUIT TRACE, SOUND BOARD #8858121



SCHEMATIC 8000188, SOUND BOARD #8858121

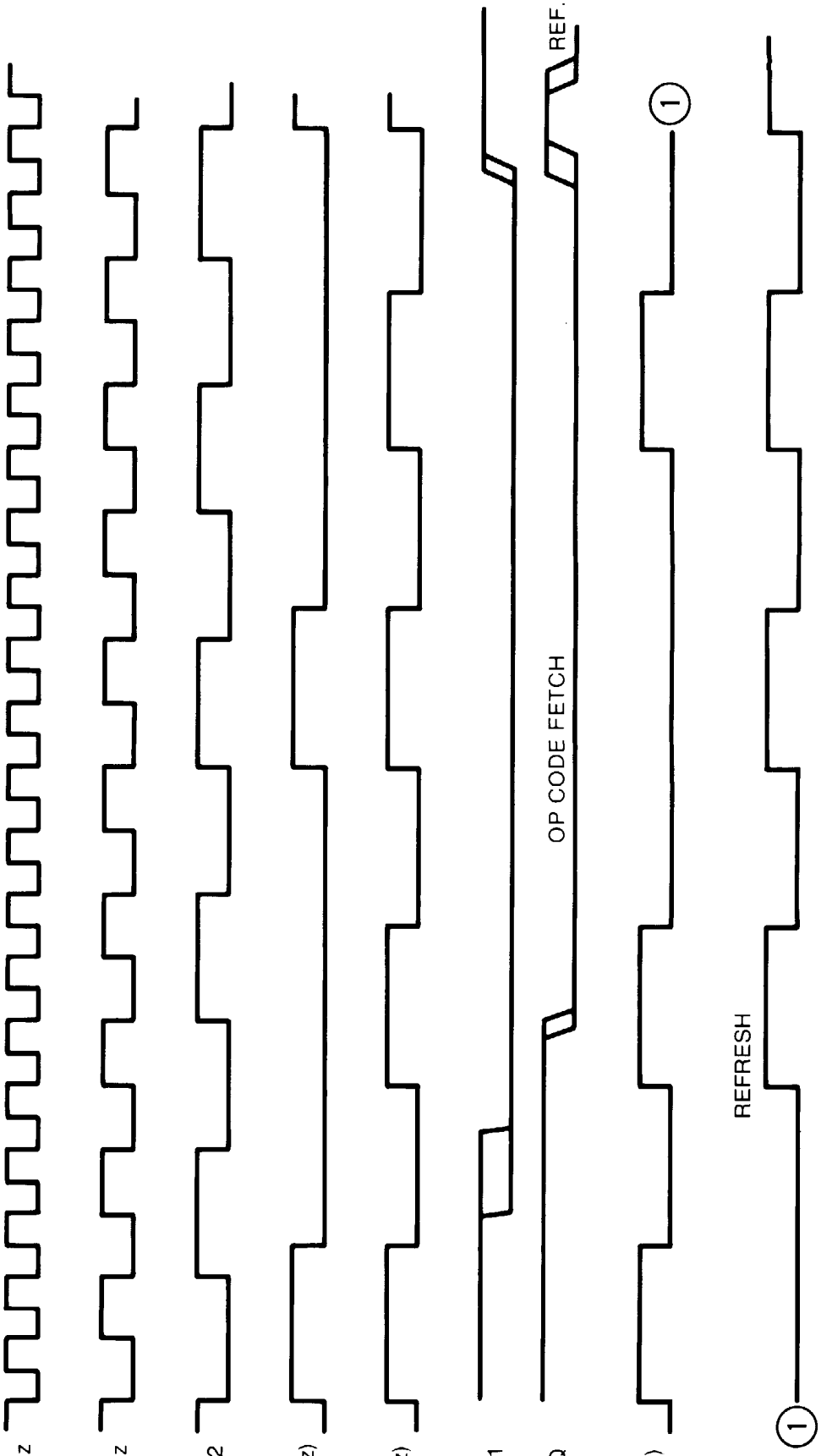


FIGURE 3-3. TIMING OF U3 & CPU

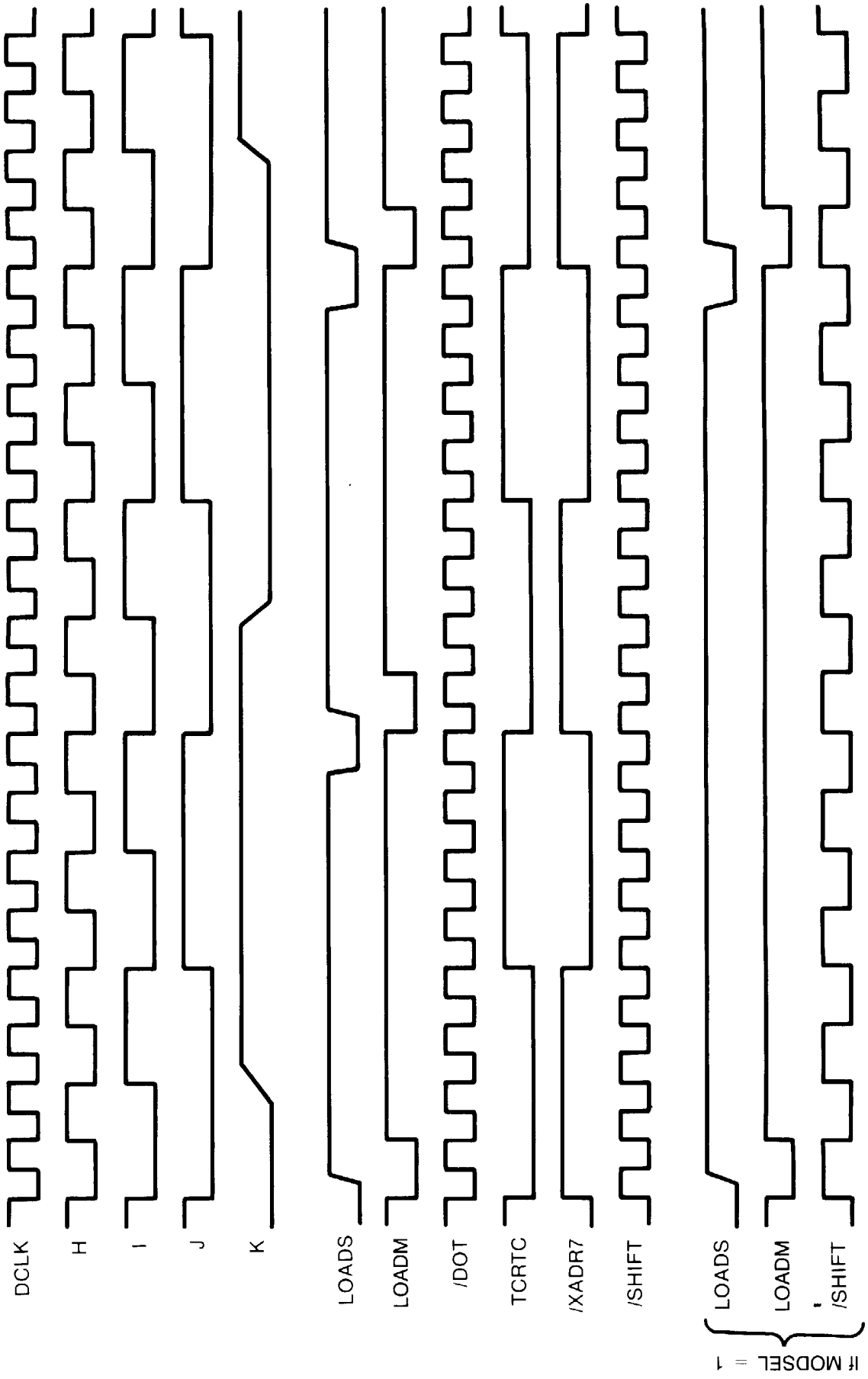


FIGURE 3-4. TIMING OF U4

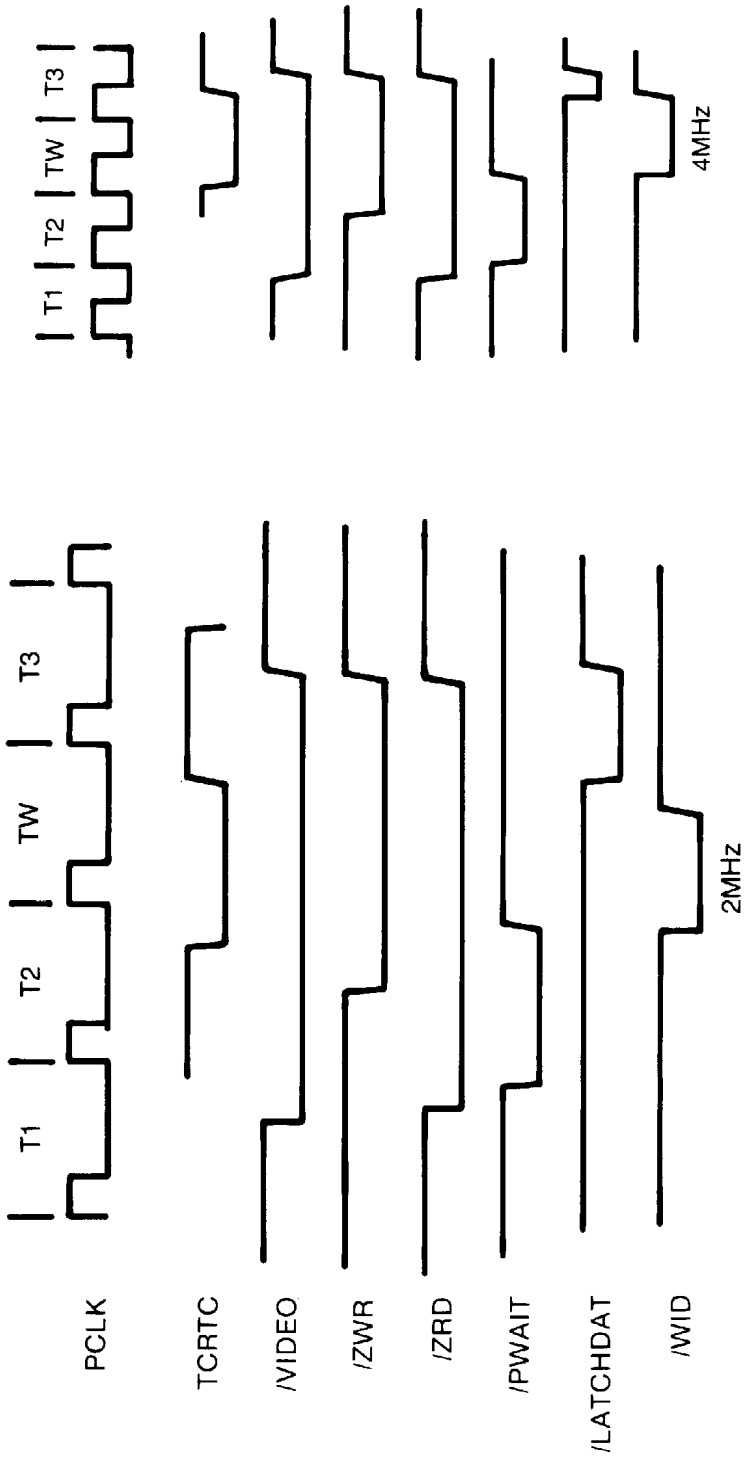


FIGURE 3-5. CPU VIDEO ACCESS TIMING

3.2 Model 4 I/O Bus

The Model 4 Bus is designed to allow easy and convenient interfacing of I/O devices to the Model 4. The I/O Bus supports all the signals necessary to implement a device compatible with the Z-80s I/O structure. That is:

Addresses:

A0 to A7 allow selection of up to 256† input and 256 output devices if external I/O is enabled.

†ports 80H to 0FFH are reserved for System use.

Data:

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus if external I/O is enabled.

Control Lines:

a. IN* - Z-80 signal specifying that an input is in progress. Gated with lORQ.

b. OUT* - Z-80 signal specifying that an output is in progress. Gated with IORQ.

c. RESET* - system reset signal.

d. IOBUSINT* - input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled.

e. IOBUSWAIT* - input to the CPU wait line allowing I/O Bus device to force wait states on the Z-80 if external I/O is enabled.

f. EXTIOSEL* - input to CPU which switches the I/O Bus data bus transceiver and allows an INPUT instruction to read I/O Bus data.

g. M1* - and IORQ* - standard Z-80 signals. . . .

The address line, data line, and control lines a to c and e to g are enabled only when the ENEXIO bit in EC is set to a one.

To enable I/O interrupts, the ENIOBUSINT bit in the CPU IOPORT E0 (output port) must be a one. However, even if it is disabled from generating interrupts, the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port).

See Model 4 Port Bit assignment for port 0FE, 0EC, and 0E0 on pages 28 and 29.

The Model 4 CPU board is fully protected from “foreign I/O devices” in that all the I/O Bus signals are buffered and can be disabled under software control. To attach and use an I/O device on the I/O Bus, certain requirements (both hardware and software) must be met.

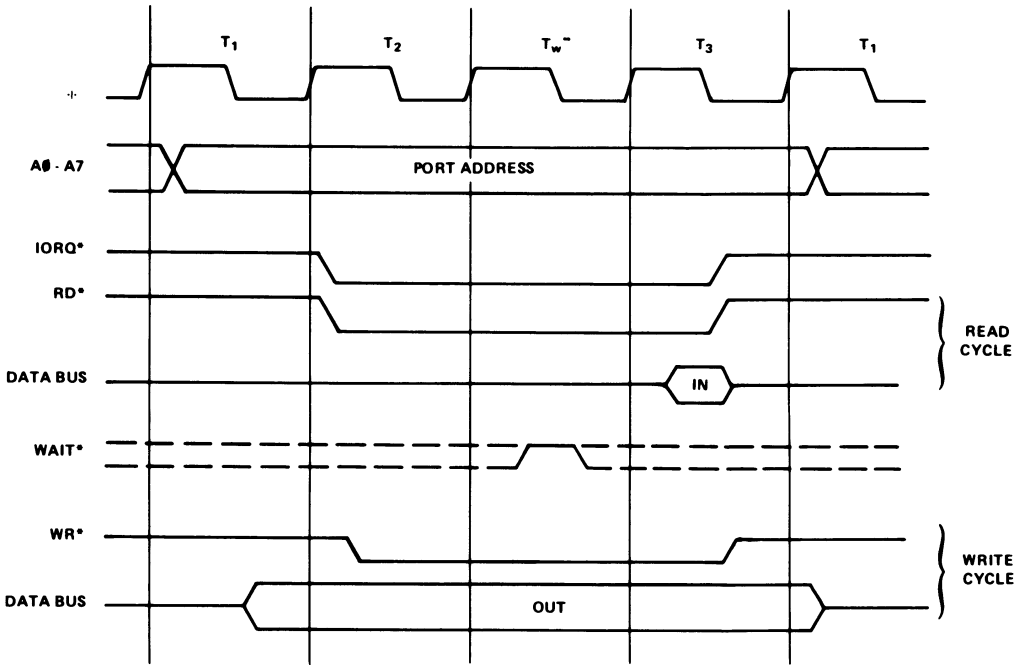
For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software. This will enable the data bus address lines and control signals to the I/O Bus edge connector. When the input device is selected, the hardware will acknowlege by asserting EXTIOSEL* low. This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines. See Figure 3.6 for the timing. EXTIOSEL* can be generated by NANDing IN and the I/O port address.

Output port device use is the same as the input port device in use, in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software - in the same fashion.

For either input or output devices, the IOBUSWAIT control line can be used in the normal way for synchronizing slow devices to the CPU. Note that since dynamic memories are used in the Model 4, the wait line should be used with caution. Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time. It is recommended that the IOBUSWAIT* line be held active no more than 500 μsec with a 25% duty cycle.

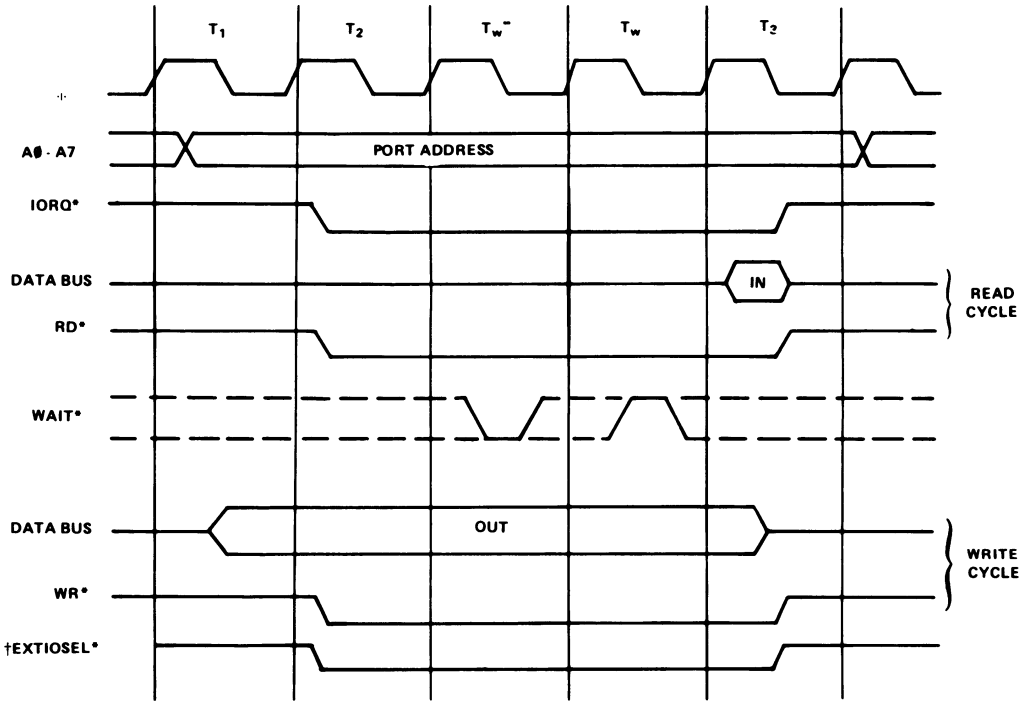
The Model 4 will support Z-80 mode 1 interrupts. A RAM jump table is supported by the LEVEL II BASIC ROMs and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F. When an interrupt occurs, the program will be vectored to the user supplied address if I/O Bus interrupts have been enabled. To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H.

Input or Output Cycles



*** Inserted by Z80 CPU**

Input or Output Cycles with Wait States.



*** Inserted by Z80 CPU**

†Coincident with IORQ* only on INPUT cycle

FIGURE 3-6. I/O BUS TIMING DIAGRAM

3.3 Model 4 Port Bits

Name: WRNMIMASKREG*
Port Address: 0E4H
Access: WRITE ONLY

Bit 7 = ENINTRO; 0 disables Disk INTRQ from generating an NMI.
1 enables above.

Bit 6 = ENDRQ; 0 disables Disk DRQ from generating an NMI.
1 enables above.

Name: RDNMISTATUS*
Port Address: 0E4H
Access: READ ONLY

Bit 7 = Status of Disk INTRQ; 1 = False, 0 = True

Bit 6 = Status of Disk DRO; 1 False, 0 = True

Bit 5 = Reset* Status; 1 = False, 0 = True

Name: MOD OUT
Port Address: 0ECH
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = Undefined

Bit 5 = DISWAIT; 0 disables video waits, 1 enables

Bit 4 = ENEXTIO; 0 disables external 10 Bus,
1 enables

Bit 3 = ENALTSET; 0 disables alternate character set,
1 enables alternate video character set.

Bit 2 = MODSEL; 0 enables 64 character mode,
1 enables 32 character mode.

Bit 1 = CASMOTORON; 0 turns cassette motor off,
1 turns cassette motor on.

Bit 0 = Undefined

Name: RDINTSTATUS*
Port Address: 0E0H
Access: READ ONLY

NOTE: A 0 indicates the device is interrupting.

Bit 7 = Undefined

Bit 6 = RS-232 ERROR INT

Bit 5 = RS-232 RCV INT

Bit 4 = RS-232 XMIT INT

Bit 3 = IOBUS INT

Bit 2 = RTC INT

Bit 1 = CASSETTE (1500 Baud) INT F

Bit 0 = CASSETTE (1500 Baud) INT R

Name: CASOUT
Port Address: 0FFH
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = Undefined

Bit 5 = Undefined

Bit 4 = Undefined

Bit 3 = Undefined

Bit 2 = Undefined

Bit 1 = Cassette output level

Bit 0 = Cassette output level

Name: WRINTMASKREG*
Port Address: 0E0H
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = ENERRORINT; 1 enables RS-232 interrupts on parity error, framing error, or data overrun error.
0 disables above.

Bit 5 = ENRCVINT; 1 enables RS-232 receive data register full interrupts,
0 disables above.

Bit 4 = ENXMITINT; 1 enables RS-232 transmitter holding register empty interrupts,
0 disables above.

Bit 3 = ENIOBUSINT; 1 enables I/O Bus interrupts,
0 disables the above.

Bit 2 = ENRTC; 1 enables real time clock interrupt,
0 disables above.

Bit 1 = ENCASINTF; 1 enables 1500 Baud falling edge interrupt,
0 disables above.

Bit 0 = ENCASINTR; 1 enables 1500 Baud rising edge interrupt,
0 disables above.

Name: CAS IN*
Port Address: 0FFH
Access: READ ONLY

Bit 7 = 500 Baud Cassette bit

Bit 6 = Undefined

Bits = DISWAIT (See Port 0ECH definition)

Bit 4 = ENEXTIO (See Port 0ECH definition)

Bit 3 = ENALTSET (See Port 0ECH definition)

Bit 2 = MODSEL (See Port 0ECH definition)

Bit 1 = CASMOTORON (See Port 0ECH definition)

Bit 0 = 1500 Baud Cassette bit

NOTE: Reading Port 0FFH clears the 1500 Baud Cassette interrupts.

Name: DRVSEL*
Port Address: 0F4H
Access: WRITE ONLY

Bit 7 = FM*/MFM; 0 selects single density,
1 selects double density.

Bit 6 = WSGEN; 0 = no wait states generated,
1 = wait states generated.

Bit 5 = PRECOMP; 0 = no write precompensation,
1 = write precompensation enabled.

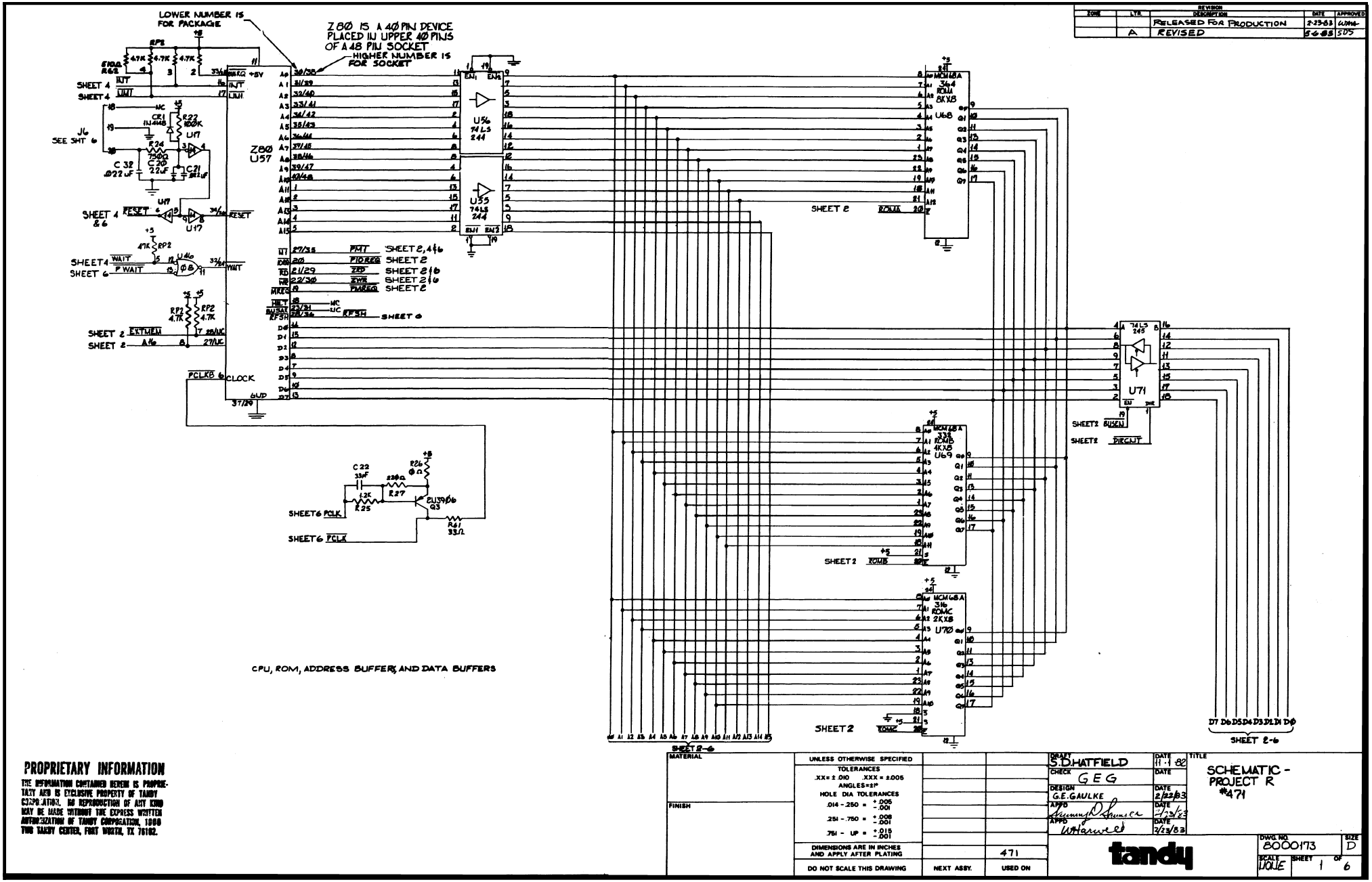
Bit 4 = SDSEL; 0 selects side 0 of diskette,
1 selects side 1 of diskette.

Bit 3 = Drive select 4

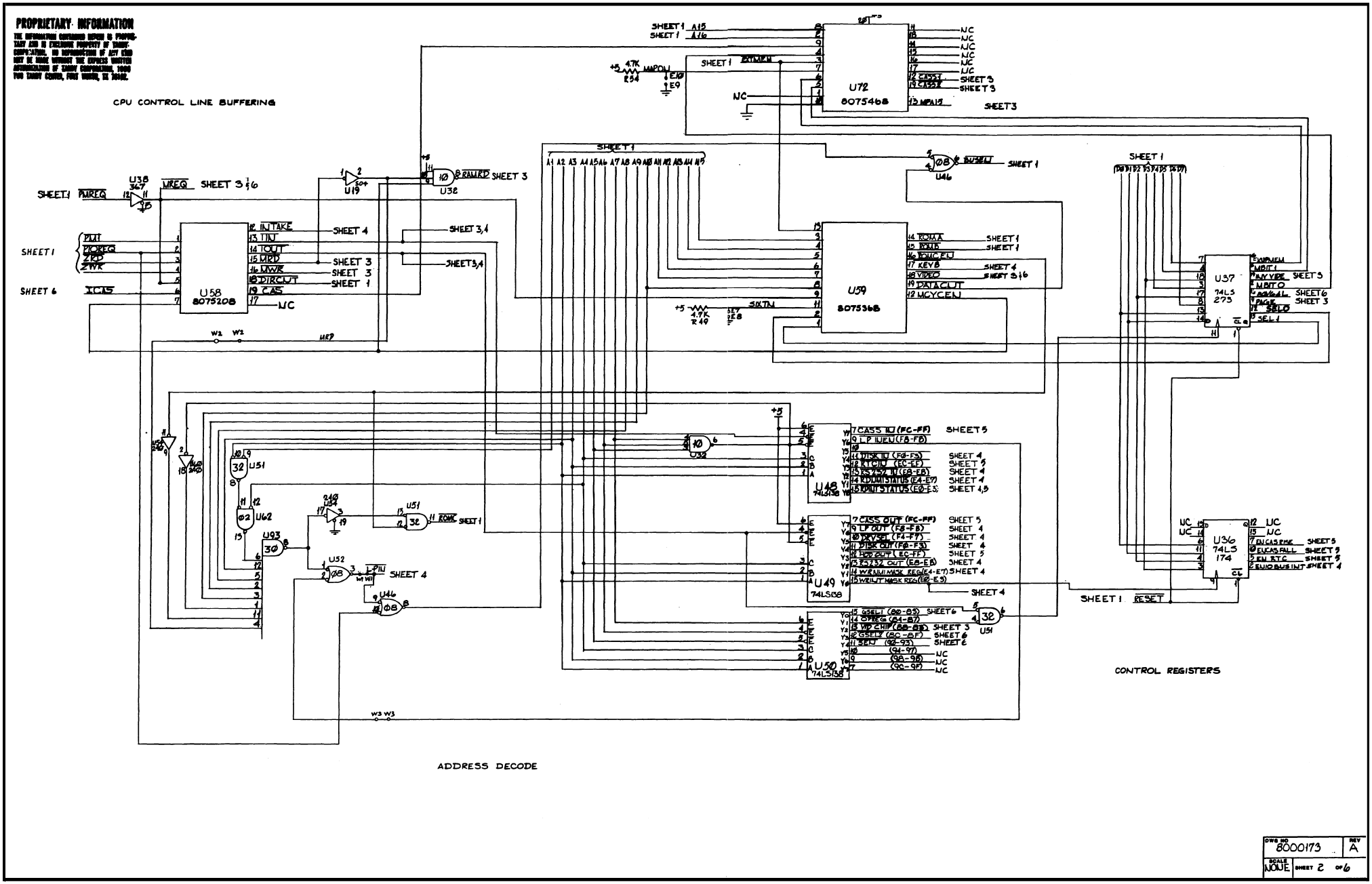
Bit 2 = Drive select 3

Bit 1 = Drive select 2

Bit 0 = Drive select 1



SCHEMATIC 8000173, 64K VERSION CPU PCB 8858090


PROPRIETARY INFORMATION
CPU CONTROL LINE BUFFERING
U72
8075468
U58
8075208
U59
8075368
U37
74LS
273
U36
74LS
174
U48
74LS138
U49
74LS138
U50
74LS138
U51
U62
U93
U32
U19
U46
U38
367
U52
U54
ADDRESS DECODE
CONTROL REGISTERS
DWG NO
8000173
REV
A
SCALE
NONE
SHEET 2 OF 6

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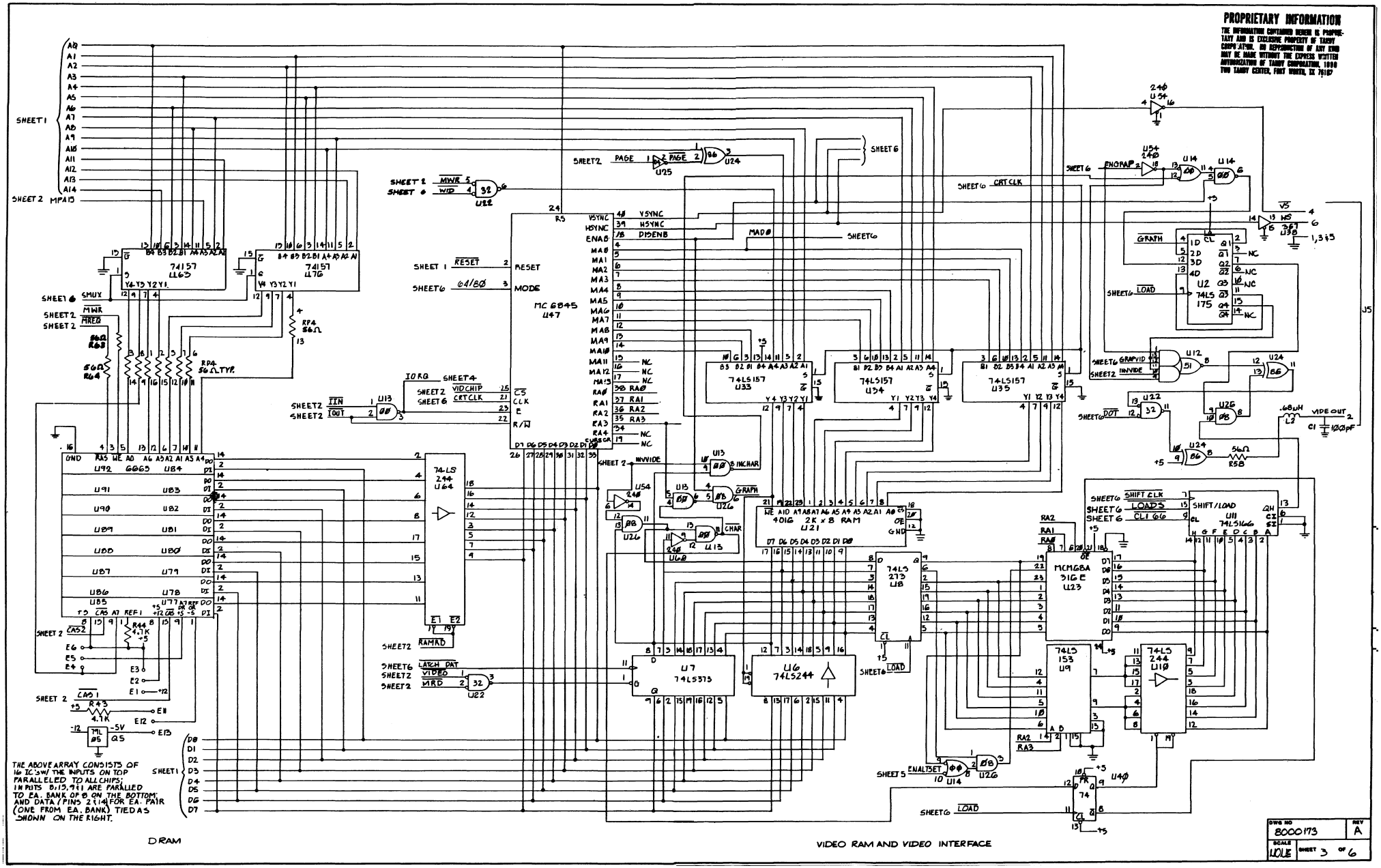

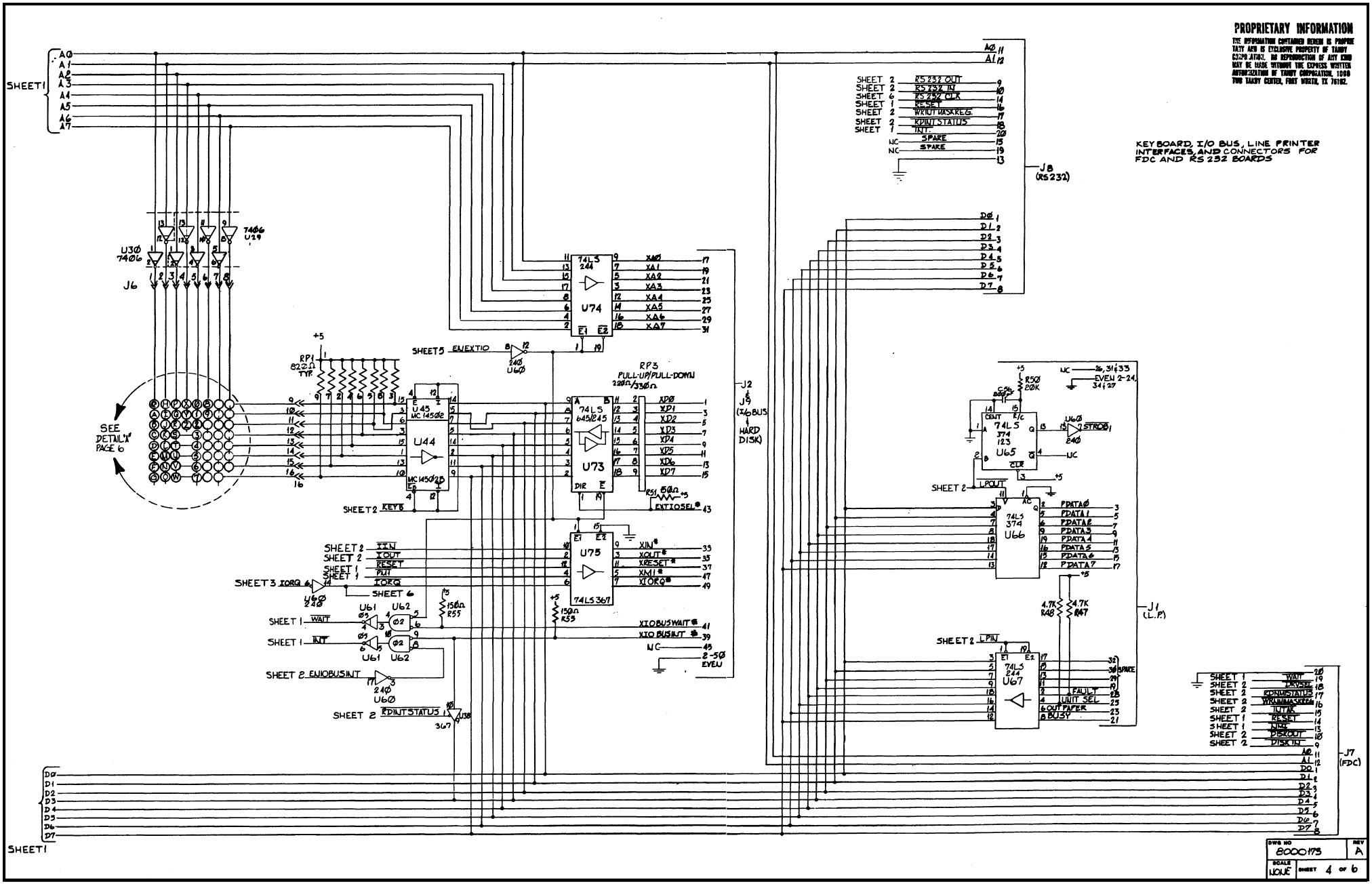
PROPRIETARY INFORMATION
KEYBOARD, I/O BUS, LINE PRINTER INTERFACES, AND CONNECTORS FOR FDC AND RS 232 BOARDS
SHEET 1
SHEET 2
SHEET 3
SHEET 5
SHEET 6
SEE DETAIL "A" PAGE 6
U30 7406
U29 7406
J6
U74 74LS 244
U44 MC 14502
U73 74LS 645/245
U75 74LS 367
U65 74LS 374 123
U66 74LS 374
U67 74LS 244
RP1 820Ω TYP.
RP3 PULL-UP/PULL-DOWN 220Ω/330Ω
J2 & J9 (I/O BUS & HARD DISK)
J8 (RS232)
J1 (L.P.)
J7 (FDC)
RS232 OUT
RS232 IN
RS232 CLK
RESET
WRINT MASKREG.
RDINT STATUS
INT.
SPARE
EXTIOSEL
IIN
IOUT
RESET
PMI
IORQ
WAIT
INT
ENIOBUSINT
RDINTSTATUS
XIN
XOUT
XRESET
XMI
XIORQ
XIOBUSWAIT
XIOBUSINT
EVEN 2-24, 31 & 33
STROB
LPOUT
LPIN
FAULT
UNIT SEL
OUT PAPER
BUSY
WAIT
DRVSEL
RDNMISTATUS
WRNMIMASKREG
INTAK
RESET
NMI
DISKOUT
DISK IN
DWG NO 8000173
REV A
SCALE NONE
SHEET 4 OF 6

PROPRIETARY INFORMATION

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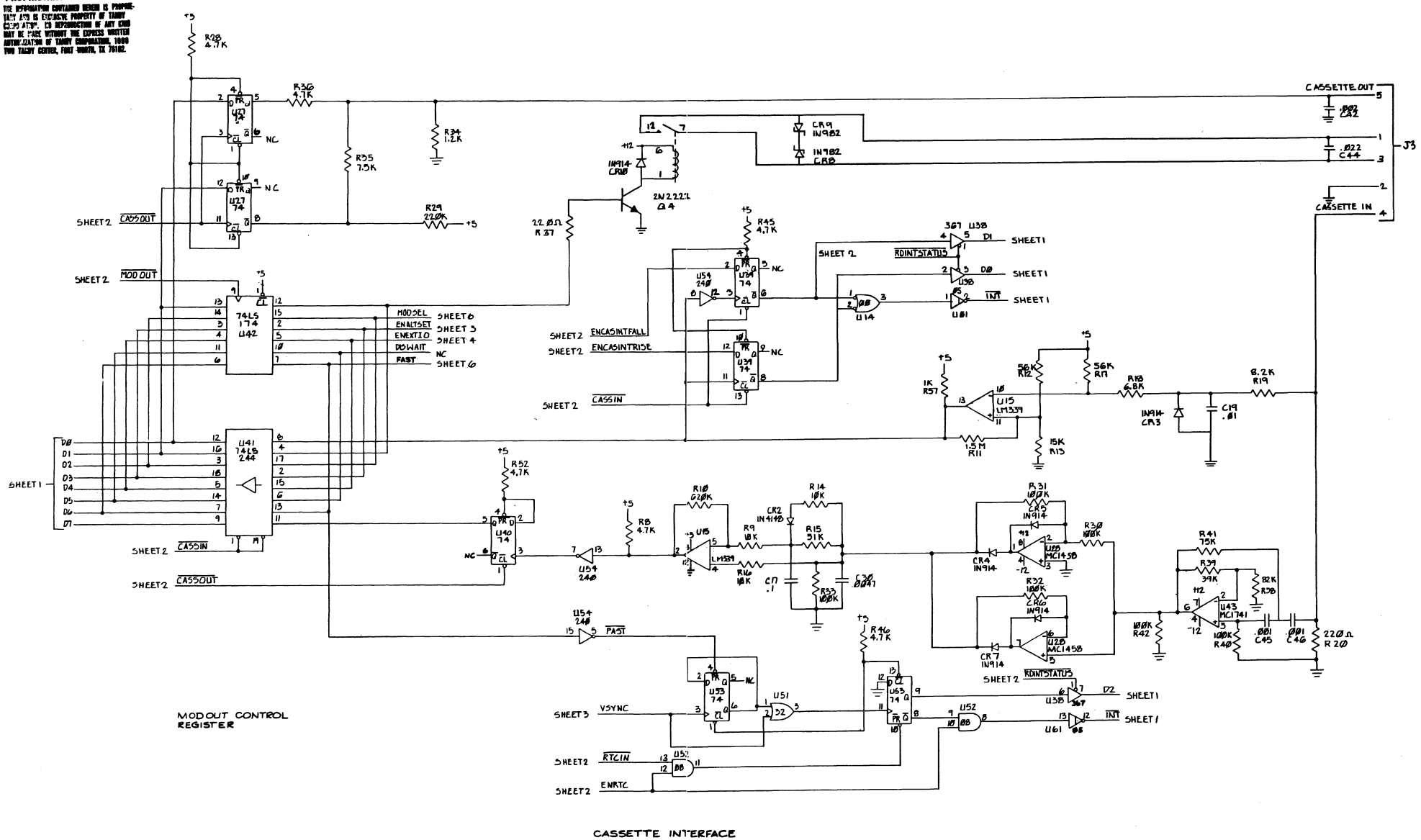

DWG NO	REV
8000173	A
SCALE NONE	SHEET 5 OF 6

PROPRIETARY INFORMATION

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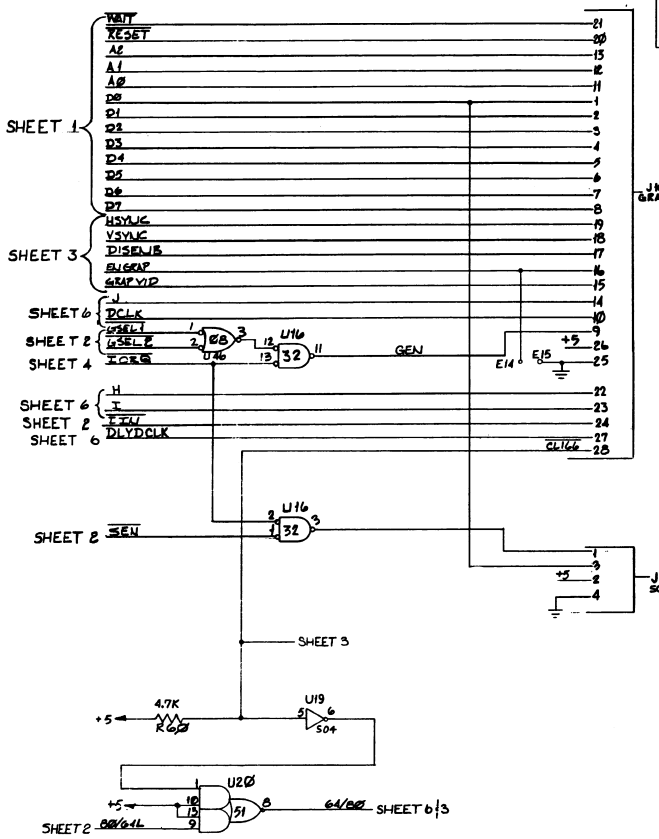
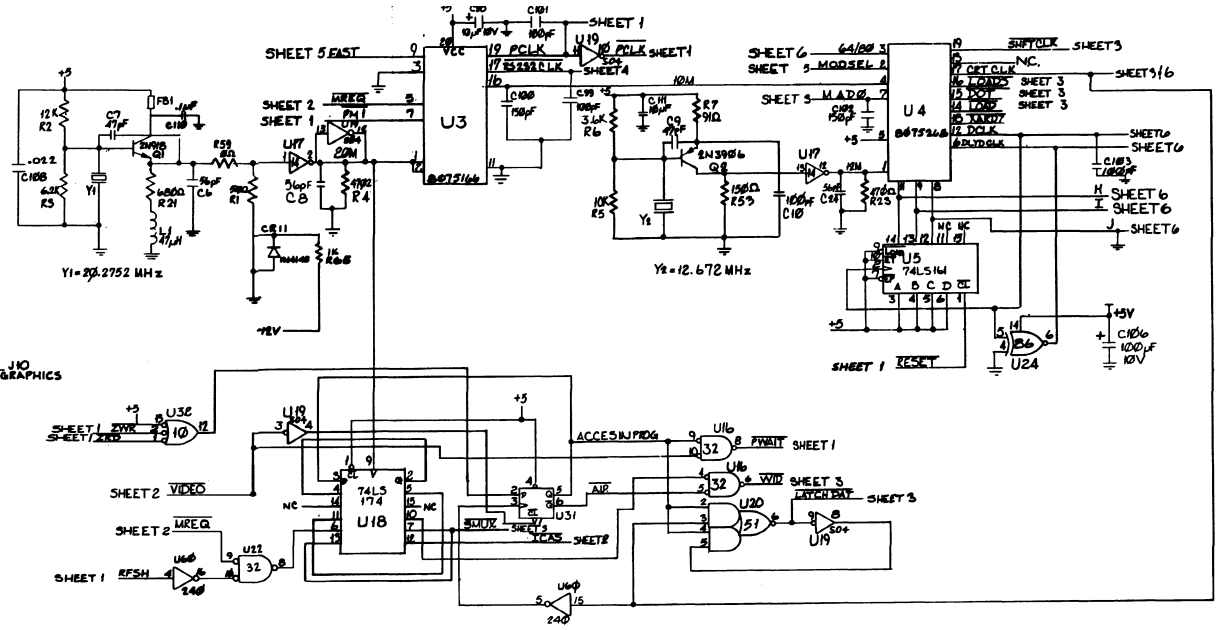
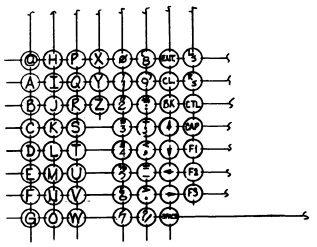


GRAPHICS AND SOUND BOARD CONNECTORS

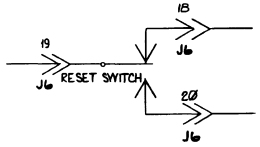


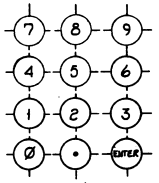
TIMING GENERATION



DETAIL "A"
FROM PAGE 4.

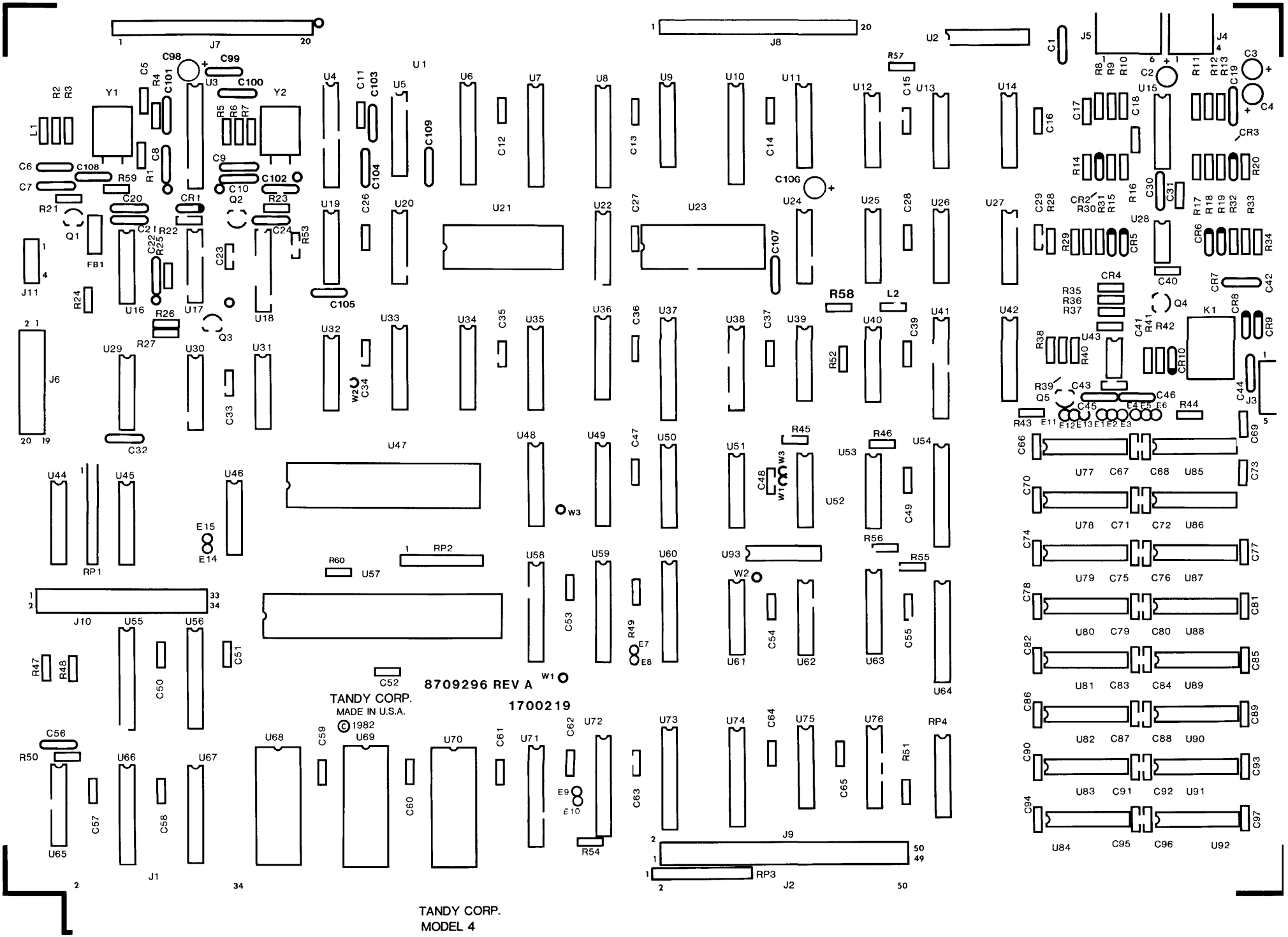
KEYBOARD DETAIL





THE ABOVE KEYS (THE NUMERIC KEYPAD) ARE CONNECTED IN PARALLEL WITH SIMILAR KEYS OF THE KEYBOARD MATRIX.

DWG NO	REV
8000173	A
SCALE NONE	SHEET 6 OF 6



CPU COMPONENT LAYOUT

Parts List, CPU PCB #6700104AA3
Model 4 16K, Cassette Input
Catalog number 26-1067

Item	Qty	Description	Mfgr's Part No.
1	4	Cap, 100 pfd 50V C. Disk (C1,99,101,103)	8301104
2	3	Cap, 10 ufd 35V Elec. Rad (C2-4)	8326103
3	74	Cap, 0.1 ufd 50v Mono Axial (C5,11-18,23,26-29,31,33-37,39-41,43,47-55, 57-97)	8374104
4	1	Cap, 56 pfd 50v C. Disk NPO (C6)	8300563
5	2	Cap, 47 pfd 50V C. Disk NPO (C7,9)	8300472
6	2	Cap, 56 pfd 50V C. Disk (C8,24)	8300564
7	1	Cap, 100 pfd 50V C. Disk (C10)	8301103
8	1	Cap, .01 ufd 50V C. Disk (C19)	8303104
9	1	Cap, 22 ufd 16V Elec. Rad(C20)	8326221
10	4	Cap, .022 ufd 50V C. Disk (C21,32,44,108)	8303224
11	1	Cap, 33 pfd 50V C. Disk (C22)	8300334
12	1	Cap, .0047 ufd 50V C. Disk (C30)	8302474
13	1	Cap, .0022 ufd 50V C. Disk (C42)	8302224
14	2	Cap, .001 ufd 50V Mono Axial (C45,46)	8372104
15	1	Cap, 200 pfd 50V (C56)	8301204
16	1	Cap, 10 ufd 10V Tant. (C98)	8336101
17	5	Cap, 150 pfd 50V C. Disk (C100,102,104,107,109)	8301154
18	1	Cap, 100 ufd 10V Tant. (C106)	8337101
19	2	Connector, 4-Pin Right Angle (J4,J11)	8519079
20	1	Connector, 5-Pin Right Angle (J3)	8519091
21	1	Connector, 6-Pin Right Angle (J5)	8519103
22	1	Connector, Dual 10 Rt. Angle Header (J6)	8519107
23	2	Connector, 20-Pin Flat Flex Cable (J7,8)	8519101
24	1	Connector, 17-Pin Dual Header (J10)	8519169
25	8	Diode, 1N4148 Zener 75V (CRl-7,l0)	8150148
26	1	Ferrite Bead (FB1)	8419014
27	1	Inductor, 47uH (L1)	8419028
28	1	Inductor, .68uH (L2)	8419029
29	1	IC, 74LS175 Quad Flip-Flop (U2)	8020175
30	1	IC, PAL16R6A (U3)	8075166
31	1	IC, PALl6L8 (U4)	8075268
32	1	IC, 74LS161 Binary Counter (U5)	8020161
33	8	IC, 74LS244 Quad Tranceiver (U6,10, 41,55,56,64,67,74)	8020244

Parts List, CPU PCB #6700104AA3
Model 4 16K, Cassette Input
Catalog number 26-1067

Item	Qty	Description	Mfgr's Part No.
34	1	IC, 74LS373 Octal Latch (U7)	8020373
35	2	IC, 74LS273 Octal Flip-Flop (U8,37)	8020273
36	1	IC, 74LS153 Dual Multiplexer (U9)	8020153
37	1	IC, 74LS166 Shift Register (Ull)	8020166
38	2	IC, 74LS51 AND OR Invert (U12,20)	8020051
39	2	IC, 74LS00 Quad 2-IN NAND (U13,14)	8020000
40	1	IC, LM339 Comparator (U15)	8050339
41	3	IC, 74LS32 Quad 2-IN OR (U16,22,51)	8020032
42	1	IC, 74LS14 Hex Inverter (U17)	8020014
43	3	IC, 74LS174 Flip-Flop (U18,36,42)	8020174
44	1	IC, 74S04 (U19)	8010004
45	1	IC, 4016 200NS RAM 2K X 8 Static (U21)	8040116
46	1	IC, MCM68A316E Character Generator (U23)	8044316
47	1	IC, 74LS86 Quad 2-IN OR (U24)	8020086
48	1	IC, 74LS04 Hex Inverter (U25)	8020004
49	3	IC, 74LS08 Quad 2-IN AND (U26,46,52)	8020008
50	5	IC, 74LS74 Dual Flip-Flop (U27,31,39,40,53)	8020074
51	1	IC, MC1458 OP-AMP (U28)	8050458
52	2	IC, 7406 Hex Inverter (U29,30)	8000006
53	1	IC, 74LS10 Triple 3-IN NAND (U32)	8020010
54	3	IC, 74LS157 Quad Multiplexer (U33-35)	8020157
55	2	IC, 74LS367 Memory (U38,75)	8020367
56	1	IC, MC1741 OP-AMP (U43)	8050741
57	2	IC, MC14502 B CMOS Driver (U44,45)	8030502
58	1	IC, SY68045 CTC 60HZ (U47)	8040045
59	3	IC, 74LS138 Decoder (U48-50)	8020138
60	2	IC, 74LS240 Octal Buffer (U54,60)	8020240
61	1	IC, Z80A CPU (U57)	8047880
62	1	IC, PAL10L8 (U58)	8075208
63	1	IC, PALl6L8 (U59)	8075368
64	1	IC, 7405 O.C. Buffer (U61)	8000005
65	1	IC, 74LS02 Quad 2-IN NOR (U62)	8020002
66	2	IC, 74157 Quad Multiplexer (U63,76)	8000157
67	1	IC, 74LS123 Dual Multivibrator (U65)	8020123
68	1	IC, 74LS374 Octal Flip-Flop (U66)	8020374
69	1	IC, MCM68A364 ROM A (U68)	8041364
70	1	IC, MCM68A332 ROM B (U69)	8040332
71	1	IC, MCM68A316 ROM C (U70)	8048316
72	2	IC, 74LS245 Octal Tranceiver (U71,73)	8020245
73	1	IC, DIP Shunt 4-POS. (U72)	8489057
74	8	IC, MCM4116 16K RAM 200NS (U77-84)	8042016
75	1	IC, 74LS30 Positive NAND (U93)	8020030

Parts List, CPU PCB #6700104AA3
Model 4 16K, Cassette Input
Catalog number 26-1067

Item	Qty	Description	Mfgr's Part No.
76	1	Relay, 12V 2 AMP (K1)	8429105
77	2	Res, 510 ohm, 5% 1/4W (R1,59)	8207151
78	1	Res, 12K ohm, 5% 1/4w (R2)	8207312
79	1	Res, 6.2K ohm, 1/4W (R3)	8207262
80	2	Res, 470 ohm, 5% 1/4w (R4,23)	8207147
81	4	Res, 10K ohm, 5% 1/4w (R5,9,14,16)	8207310
82	1	Res, 3.6K ohm, 5% 1/4w (R6)	8207236
83	1	Res, 91 ohm, 5% (R7)	8207091
84	13	Res, 4.7K ohm, 5% 1/4W (R8,28,36,43-49,52,54,60)	8207247
85	1	Res, 620K ohm, 5% 1/4W (R10)	8207462
86	1	Res, 1.5M ohm, 5% 1/4W (R11)	8207515
87	2	Res, 56K ohm, 5% 1/4W (R12,17)	8207356
88	2	Res, 15K ohm, 5% 1/4W (R13)	8207315
89	1	Res, 51K ohm, 5% 1/4W (R15)	8207351
90	1	Res, 6.8K ohm, 5% 1/4W (R18)	8207268
91	1	Res, 8.2K ohm, 5% 1/4w (R19)	8207282
92	3	Res, 220 ohm, 5% 1/4W (R20,27,37)	8207122
93	1	Res, 680 ohm, 5% 1/4W (R21)	8207168
94	7	Res, l00K ohm, 5% 1/4W (R22,30-33,40,42)	8207410
95	1	Res, 750 ohm, 5% 1/4w (R24)	8207175
96	2	Res, 1.2K ohm, 5% 1/4W (R25,34)	8207212
97	1	Res, 22 ohm, 5% 1/4W (R26)	8207022
98	1	Res, 220K ohm, 5% 1/4W (R29)	8207422
99	1	Res, 7.5K ohm, 5% 1/4W (R35)	8207275
100	1	Res, 82K ohm, 5% 1/4w (R38)	8207382
101	1	Res, 39K ohm, 5% 1/4W (R39)	8207339
102	1	Res, 75K ohm, S% 1/4W (R41)	8207375
103	1	Res, 20K ohm, 5% 1/4W (R50)	8207320
104	4	Res, 150 ohm, 5% 1/4W (R51,53,55,56)	8207150
105	1	Res, 1K ohm, 5% 1/4W (R57)	8207210
106	1	Res, 56 ohm, 5% 1/4W (R58)	8207056
107	1	Res Pak, 820 ohm, SIP 10-PIN (RP1)	8290182
108	1	Res pak, 4.7K ohm, SIP 8-PIN (RP2)	8292246
109	1	Res Pak, 27 ohm, DIP 16-PIN (RP4)	8290027
110	1	Transistor, 2N918 (Ql)	8110918
111	2	Transistor, 2N3906 PNP (Q2,3)	8100906
112	1	Transistor, 2N2222 (Q4)	8110222
		MISCELLANEOUS	
113	1	Crystal, 20.2752 MHz (Y1)	8409031
114	1	Crystal, 12.672 MHz (Y2)	8409030

Parts List, CPU PCB #6700104AA3
Model 4 16K, Cassette Input
Catalog number 26-1067

Item	Qty	Description	Mfgr's Part No.
115	3	Jumper Wire 20 Gauge (W1-3)	*NOTE
116	1	PCB Logic Board, Rev. PP3	8709296
117	1	Regulator, 79LO5, -5V (Q5)	8051905
118	7	Socket, 20-Pin DIP (U3,4,58,59,71-73)	8509009
119	5	Socket, 24-Pin DIP (U21,23,68-70)	8509001
120	2	Socket, 40-Pin DIP (U47,57)	8509002
121	16	Socket, 16-Pin DIP (U77-84,85-92)	8509003
122	13	Staking Pin (E1-8,11-15)	8529014

Note: W1,W3 are 4-1/2" long, W2 is 6" long

Parts List, CPU PCB 8858090
Model 4 64K, Single or Double Drive
Catalog Number 26-1068 or 26-1069

Item	Qty	Description	Mfgr's Part No.
1	4	Cap, 100 pfd 50V C. Disk (C1,99,101,103)	8301104
2	3	Cap, 10 MFD 35V ELEC. RAD (C2-4)	8326103
3	58	Cap, 0.1MFD 50V MONO AXIAL (C5,11-18,23,26-29,31,33-37,39-41,43, 47-55,57-65,67,69,71,73,75,77,79,81,83, 85,87,89,91,93,95,97)	8374104
4	1	Cap, 56 PFD 50V C. DISK NPO (C6)	8300563
5	2	Cap, 47 PFD 50V C. DISK NPO (C7,9)	8300472
6	2	Cap, 56 PFD 50V C. DISK (C8,24)	8300564
7	1	Cap, 100 PFD 50V C. DISK (C10)	8301103
8	1	Cap, .01 MFD 50V C. DISK (C19)	8303104
9	1	Cap, 22 MFD 16V ELEC. RAD(C20)	8326221
10	4	Cap, .022 MFD 50V C. DISK (C21,32,44,108)	8303224
11	1	Cap, 33 PFD 50V C. DISK (C22)	8300334
12	1	Cap, .0047 MFD 50V C. DISK (C30)	8302474
13	1	Cap, .0022 MFD 50V C. DISK (C42)	8302224
14	2	Cap, .001 MFD 50V MONO AXIAL (C45,46)	8372104
15	1	Cap, 200 PFD 50V (C56)	8301204
16	1	Cap, 10 MFD 10V TANT. (C98)	8336101
17	5	Cap, 150 PFD 50V C. DISK (C100,102,104,107,109)	8301154
18	1	Cap, 100 MFD 10V TANT. (C106)	8337101
19	2	Connector, 4-Pin Right Angle (J4,J11)	8519079
20	1	Connector, 5-Pin Right Angle (J3)	8519091
21	1	Connector, 6-Pin Right Angle (J5)	8519103
22	1	Connector, Dual 10 Rt. Angl. Header (J6)	8519107
23	2	Connector, 20-Pin Flat Flex Cable (J7,8)	8519101
24	1	Connector, 17-Pin Dual Header (J10)	8519169
25	8	Diode, 1N4148 Zener 75V (CR1-7,10)	8150148
26	1	Ferrite Bead (FB1)	8419014
27	1	Inductor, 47uH (L1)	8419028
28	1	Inductor, .68uH (L2)	8419029
29	1	IC, 74LS175 Quad Flip-Flop (U2)	8020175
30	1	IC, PAL16R6A (U3)	8075166
31	1	IC, PALl6L8 (U4)	8075268
32	1	IC, 74LS161 Binary Counter (U5)	8020161
33	8	IC, 74LS244 Quad Tranceiver (U6,l0,41,55,56,64,67,74)	8020244
34	1	IC, 74LS373 Octal Latch (U7)	8020373
35	2	IC, 74LS273 Octal Flip-Flop (U8,37)	8020273
36	1	IC, 74LS153 Dual Multiplexer (U9)	8020153

Parts List, CPU PCB 8858090
Model 4 64K, Single or Double Drive
Catalog Number 26-1068 or 26-1069

Item	Qty	Description	Mfgr's Part No.
37	1	IC, 74LS166 Shift Register (Ull)	8020166
38	2	IC, 74LS51 AND OR Invert (U12,20)	8020051
39	2	IC, 74LS00 Quad 2-In NAND (U13,14)	8020000
40	1	IC, LM339 Comparator (U15)	8050339
41	3	IC, 74LS32 Quad 2-In OR (U16,22,51)	8020032
42	1	IC, 74LS14 Hex Inverter (U17)	8020014
43	3	IC, 74LS174 Flip-Flop (U18,36,42)	8020174
44	1	IC, 74S04 (U19)	8010004
45	1	IC, 4016 200NS RAM 2K X 8 Static (U21)	8040116
46	1	IC, MCM68A316E Character Generator (U23)	8044316
47	1	IC, 74LS86 Quad 2-In OR (U24)	8020086
48	1	IC, 74LS04 Hex Inverter (U25)	8020004
49	3	IC, 74LS08 Quad 2-In AND (U26,46,52)	8020008
50	5	IC, 74LS74 Dual Flip-Flop (U27,31,39,40,53)	8020074
51	1	IC, MC1458 OP-AMP (U28)	80504S8
52	2	IC, 7406 Hex Inverter (U29,30)	8000006
53	1	IC, 74LS10 Triple 3-In NAND (U32)	8020010
54	3	IC, 74LS157 Quad Multiplexer (U33-35)	8020157
55	2	IC, 74LS367 Memory (U38,75)	8020367
56	1	IC, MC1741 OP-AMP (U43)	8050741
57	2	IC, MC14502 B CMOS Driver (U44,45)	8030502
58	1	IC, SY68045 CTC 50Hz Version (U47)	8041045
59	3	IC, 74LS138 Decoder (U48-50)	8020138
60	2	IC, 74LS240 Octal Buffer (U54,60)	8020240
61	1	IC, Z80A CPU (U57)	8047880
62	1	IC, PAL10L8 (U58)	8075208
63	1	IC, PALl6L8 (U59)	8075368
64	1	IC, 7405 O.C. Buffer (U61)	8000005
65	1	IC, 74LS02 Quad 2-In NOR (U62)	8020002
66	2	IC, 74157 Quad Multiplexer (U63,76)	8000157
67	1	IC, 74LS123 Dual Multivibrator (U65)	8020123
68	1	IC, 74LS374 Octal Flip-Flop (U66)	8020374
69	1	IC, MCM68A364 ROM A (U68)	8048364
70	1	IC, MCM68A332 ROM B (U69)	8040332
71	1	IC, MCM68A316 ROM C (U70)	8042316
72	2	IC, 74LS245 Octal Tranceiver (U71,73)	8020245
73	1	IC, DIP Shunt 4-Pos. (U72)	8489057
74	8	IC, MCM6665 64K RAM 200NS (U85-92)	8040665
75	1	IC, 74LS30 Positive NAND (U93)	8020030
76	1	Relay, 12V 2 Amp (Kl)	8429105
77	2	Res, 510 ohm, 5% 1/4W (R1,59)	8207151
78	1	Res, 12K ohm, 5% 1/4W (R2)	8207312
79	1	Res, 6.2K ohm, 1/4W (R3)	8207262
80	2	Res, 470 ohm, 5% 1/4W (R4,23)	8207147

Parts List, CPU PCB 8858090
Model 4 64K, Single or Double Drive
Catalog Number 26-1068 or 26-1069

Item	Qty	Description	Mfgr's Part No.
81	4	Res, 10K ohm, 5% 1/4w (R5,9,14,16)	8207310
82	1	Res, 3.6K ohm, 5% 1/4W (R6)	8207236
83	1	Res, 91 ohm, 5% (R7)	8207091
84	13	Res, 4.7K ohm, 5% 1/4W (R8,28,36,43-49,52,54,60)	8207247
85	1	Res, 620K ohm, 5% 1/4W (R10)	8207462
86	1	Res, 1.5Meg ohm, 5% 1/4W (R11)	8207515
87	2	Res, 56K ohm, 5% 1/4W (R12,17)	8207356
88	2	Res, 15K ohm, 5% 1/4W (R13)	8207315
89	1	Res, 51K ohm, 5% 1/4W (R15)	8207351
90	1	Res, 6.8K ohm, 5% 1/4W (R18)	8207268
91	1	Res, 8.2K ohm, 5% 1/4W (R19)	8207282
92	3	Res, 220 ohm, 5% 1/4W (R20,27,37)	8207122
93	1	Res, 680 ohm, 5% 1/4W (R21)	8207168
94	7	Res, l00K ohm, 5% 1/4W (R22,30-33,40,42)	8207410
95	1	Res, 750 ohm, 5% 1/4W (R24)	8207175
96	2	Res, 1.2K ohm, 5% 1/4W (R25,34)	8207212
97	1	Res, 22 ohm, 5% 1/4W (R26)	8207022
98	1	Res, 220K ohm, 5% 1/4W (R29)	8207422
99	1	Res, 7.5K ohm, 5% 1/4W (R35)	8207275
100	1	Res, 82K ohm, 5% 1/4W (R38)	8207382
101	1	Res, 39K ohm, 5% 1/4W (R39)	8207339
102	1	Res, 75K ohm, 5% 1/4W (R41)	8207375
103	1	Res, 20K ohm, 5% 1/4W (R50)	8207320
104	4	Res, 150 ohm, 5% 1/4W (R51,53,55,56)	8207150
105	1	Res, 1K ohm, 5% 1/4W (R57)	8207210
106	1	Res, 56 ohm, 5% 1/4W (R58)	8207056
107	1	Res Pak, 820 ohm, SIP 10-Pin (RP1)	8290182
108	1	Res Pak, 4.7K ohm, SIP 8-Pin (RP2)	8292246
109	1	Res Pak, 27 ohm, DIP 16-Pin (RP4)	8290027
110	1	Transistor, 2N918 (Q1).	8110918
111	2	Transistor, 2N3906 PNP (Q2,3)	8100906
112	1	Transistor, 2N2222 (Q4)	8110222
		MISCELLANEOUS	
113	1	Crystal, 20.2752 MHz (Y1)	8409031
114	1	Crystal, 12.672 MHz (Y2)	8409030
115	3	Jumper Wire, 20 Gauge (W1-3)	*NOTE
116	1	PCB, Logic Board Rev. PP3	8709296
117	7	Socket, 20-Pin DIP (U3,4,58,59,71-73)	8509009
118	5	Socket, 24-Pin DIP (U21,23,68-70)	8509001
119	2	Socket, 40-Pin DIP (U47,57)	8509002
120	16	Socket, 16-Pin DIP (U77-84,85-92)	8509003
121	10	staking Pin (El-8,11-15)	8529014

SECTION IV

FLOPPY DISK INTERFACE

FLOPPY DISK INTERFACE

4.1 Model 4 FDC PCB #8858060

The TRS-80 Model 4 Floppy Disk interface Board is an optional board which if incorporated provides a standard five inch floppy disk controller. The Floppy Disk Interface Board supports both single and double density encoding schemes. This feature, along with a special software package, allows the transfer of Model I disk files to the Model 4 system. Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one. The amount of write precompensation is continuously variable from 0 nsec to more than 500 nsec. The write pre-compensation is factory adjusted to 200 nsec. The data clock recovery logic incorporates a phaselocked loop oscillator Which achieves state-of-the-art reliability. One to four drives may be controlled by the interface (two internal drives and two external). All data transfers are accomplished by CPU data requests. In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip. The end of the data transfer is indicated by generating a non-maskable interrupt from the interrupt request output of the FDC chip. A hardware watchdog timer insures that error conditions will not hang the wait line to the CPU for a period long enough to destroy RAM contents.

4.1.1 Control and Data Buffering

Refer to the Schematic Diagram 8000095.

The Floppy Disk Controller Board is an I/O port mapped device which utilizes ports E4H, F0H, F1H, F2H, F3H, and F4H. The decoding logic is implemented on the CPU board. (See the Decoding Logic section of the CPU discussion.) U4 of the Floppy Disk Controller Board is a non-inverting octal buffer which isolates and buffers the required control signals. Table 4-1 and Table 4-2 summarize the port and bit allocation for the Floppy Controller Board. U2 of the Floppy Disk Controller Board is a bi-directional, 8-bit transceiver used to buffer data to and from the Floppy Controller Board. The direction of data transfer is controlled by the combination of control signals DISKIN* and RDNMIMASKREG*. If either signal is active (logic low), U2 is enabled to drive data onto the CPU board data bus. If both signals are inactive (logic high), U2 is enabled to receive data from the CPU data bus.

4.1.2 Nonmaskable Interrupt Logic

A dual “D” flip-flop (U5) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMIMASREG*. The outputs of US control the conditions which will generate a non-maskable interrupt to the CPU. The NMI-interrupt conditions are programmed by doing an OUT instruction to port E4H with the appropriate bits set. If data bit 7 is set, an NMI will be generated by an FDC interrupt request. If data bit 7 is reset, interrupt requests from the FOG are disabled. If data bit 6 is set, an NMI will be generated by Motor Time Out. If data bit 6 is reset, interrupts on Motor Time Out are disabled. An IN instruction from port E4H enables the CPU to question the Floppy Disk Controller Board to determine the source of the non-maskable interrupt. Data bit 7 indicates the status of FOG interrupt request (0 = true, 1 = false). Data bit 6 indicates the status of Motor Time Out (0 = true, 1 = false). Data bit 5 indicates the status of the front panel reset (0 = true, 1 = false). The control signal RDNMIMASKREG* when active (logic 0), gates this status onto the CPU data bus.

4.1.3 Drive Select Latch and Motor On Logic

Selecting a drive prior to a disk I/O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set. The following table describes the bit allocation of the Drive Select Latch.

DATA BIT	FUNCTION
D0	Selects Drive 0 when set *
D1	Selects Drive 1 when set *
D2	Selects Drive 2 when set *
D3	Selects Drive 3 when set *
D4	Side 0 selected when reset, side 1 selected if set
D5	Write Precom. engaged when set, disabled if reset
D6	Generate waits if set, no waits if reset
D7	Selects MFM mode if set, FM mode if reset

*Only one of these bits should be set per output.

Table 4.1. Port F4H Bit Allocation

A hex “0” flip-flop (U6) latches the drive select bits, side select and FM*/MFM bits on the rising edge of the control signal IDRVSEL*. A dual “D” flip-flop (U18) is used to latch the Wait Enable and Precompensation enable bits on the rising edge of IDRVSEL*. The rising edge of IDRVSEL* also triggers a one-shot (1/2 of U15) which produces a Motor On to the disk drives. The duration of the Motor On signal is approximately two seconds. The spindle motors are not designed for continuous operation, therefore the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected. The Motor On one-shot is retriggerable by simply executing an OUT instruction to the Drive Select Latch.

4.1.4 Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an output to the Drive Select Latch with D6 set. Pin 5 of U18 will go high after this operation. This signal is inverted by 1/6 of U1 and is routed to the CPU board where it forces the Z-80 into a wait state. The Z-80 will remain in the wait state as long as WAIT* is low. Once initiated, the wait state will remain until one of four conditions are satisfied. One half of U10 (a five input NOR gate) is used to perform this function. INTRQ, DRQ, RESET, and WAITIMOUT are the inputs to the NOR gate. If any one of these inputs are active (logic high), the output of the NOR gate (U10 pin 6) will go low. This output is tied to the clear input of the wait latch. This signal, when low, will clear the Q output (U18 pin 5) and set the Q* output (U18 pin 6). This condition causes WAIT* to go high and allows the Z-80 to exit the wait state. U20 is a 12-bit binary counter which serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents. The counter is clocked by a 1MHz signal and is enabled to count when its reset pin is low (U20 pin 11). A logic high on U20 pin 11 resets the counter ouputs. U20 pin 15 is the divide by 1024 output and is used to generate the signal WAITIMOUT. This watchdog timer logic will limit the duration of a wait to l024µsec, even if the FDC chip fails to generate a data request or an interrupt request.

4.1.5 Clock Generation Logic

A 4MHz crystal oscillator and a divide by 2 and divide by 4 counter generate the clock signals required by the FDC board. The basic 4MHz oscillator is implemented with two invertors (1/3 of U25) and a quartz crystal (Y1). One half of U24 is used to divide the basic 4MHz clock by 2 to produce a 2MHz output at U24 pin 6. This output is again divided by 2 using the remaining half of U24 to produce a 1 MHz output at U24 pin 8. The 1MHz clock is used to drive the clock input of the 1793 FDC chip and the clock input of the watchdog time (U20).

4.1.6 Disk Bus Selector Logic

As mentioned previously, the Model 4 Floppy Disk Board supports up to four drives (two internal, two external). This function is implemented by using two disk drive interface buses, one for the internal drives and one for the external drives. J4 is the edge connector used for the internal drives and J1 is the edge connector for the external drives. U22 (a quad 2 to 1 data selector) is used to select which set of inputs from the disk drive buses are routed to the 1793 FDC chip. U22 pin 1 is the control pin for the data selector. If U22 pin 1 is low, the external inputs are selected, otherwise the internal inputs are selected. This control signal (labeled EXTSEL*) is derived from the outputs of the Drive Select Latch. If Drive 2 or Drive 3 is selected, U17 pin 1will go low indicating that an external drive is selected. One half of U10 (a five input NOR gate) is used to detect when one of the four drives is selected. The output of this NOR gate (U10 pin 5) is inverted and is used as the head load timing and ready signal for the 1793 FDC chip. Therefore if any drive is selected, the head is assumed to be loaded and the selected drive is assumed to be ready.

4.1.7 Read/Write Data Pulse Shaping Logic

Two one-shots (1/2 of U15 and 1/2 of U23) are used to insure that the read and write data pulses are approximately 450nsec in duration.

4.1.8 Disk Bus Output Drivers

High current open collector drivers (U21, U9, and U1) are used to buffer the output signals from the Drive Select Latch and the FDC chip to the floppy disk drives. Note from the schematic that each output signal to the drives has two buffers associated with each signal, one set is used for the internal drive bus and the other set is used for the external bus. No select logic is required for these output signals since the drive select bits define which drive is active.

4.1.9 Write Precompensation and Clock Recovery Logic

The Write Precompensation and Read Clock Recovery logic is comprised of U11 (WD1691), U13 (WD2143) and U14 (LS629), along with a few passive components. The WD1691 is an LSI device which minimizes the external logic required to interface the 1793 FDC chip to a disk drive. With the use of an external VCO, U14, theWDl69l will derive the RCLK signal for the 1793, while providing an adjustment signal for the VCO, to keep the RCLK synchronous with the read data from the drive. Write precompensation control signals are also provided by the WD1691 to interface directly to the WD2143 (U13) clock generator. The Read Clock Recovery section of the WD1691 has five inputs: DDEN, VCO, RDD*, WG, and VFOE*/WF. It also has three outputs: PU, PD*, and RCLK. The inputs VFOE*/WF and WG when both are low, enable the Clock Recovery logic. When WG is high, a write operation is in progress and the Clock Recovery circuits are disabled regardless of the state of any other inputs.

The Write Precompensation section of the WD1691 was designed to be used with the WD2143 clock generator. Write Precompensation is not used in single density mode and the signal DDEN* when high indicates this condition. In double density mode (DDEN* = 0), the signals EARLY and LATE are used to select a phase input (01 - 04) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143 to start its pulse generation.

02 is used as the write data pulse on nominal (EARLY = 0 LATE = 0). 01 is used for the early, and 03 is used for the late. The leading edge of 04 resets the STB line in anticipation of the next write data pulse. When TG43 = 0 or DDEN* = 1, precompensation is disabled and any transitions on the WDIN line will appear on the WDOUT line.

When VFOE*/WF and WG are low, the Clock Recovery circuits are enabled. When the RDD* line goes low, the PU or PD* signals will become active. If the RDD* has made its transition in the beginning of the RCLK window, PU will go from a high impedence state to a logic one, requesting an increase in VCO frequency. If the RDD* line has made it transition at the end of the RCLK window, PU will remain in the high impedence state while PD* will go to a logic zero, requesting a decrease in the VCO frequency. When the leading edge of RDD* occurs in the center of the RCLK window, both PU and PD* will remain in the high impedence state, indicating that no adjustment of the VCO frequency is required. By tying PU and PD* together, an adjustment signal is created which will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider using R7, R10, and R9 is used to adjust the tri-state level at approximately 1.4V. This adjustment results in a worst case voltage swing of plus or minus 1V, which is acceptable for the frequency control input of the VCO (U14). This signal derived from the combination of PU and PD* will eventually correct the VCO input to exactly the same frequency multiple as the FDD* signal. The leading edge of the RDD* signal will then occur in the exact center of the RCLK window, an ideal condition for the 1793 internal recovery circuits.

4.1.10 Floppy Disk Controller Chip

The 1793 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation. The 1793 is functionally identical to the 1791 used on the Model II FDC Printer Interface Board, except that the data bus is true as opposed to inverted. Refer to the appendix section for more information on the FD1793. The Model II Technical Reference Manual also contains a good presentation of the 1791 FDC chip as well as a discussion on Write Precompensation. The following port addresses are assigned to the internal registers of the 1793 FDC chip.

PORT#	FUNCTION	
F0H	Command/Status	Register
F1H	Track	Register
F2H	Sector	Register
F3H	Data Register	

Table 4.2 Port Allocation

4.1.11 Adjustments and Jumper Options

The Data Separator must be adjusted with the 1793 in an idle condition (no command currently in operation). Adjust R7 potentiometer for a 1.4V level on pin 2 of U14. Then adjust R6 potentiometer to yield a 2MHz square wave at pin l6 of U11.

The Write Precompensation must be adjusted while executing a continuous write command on a track greater than twenty-one. Adjust R5 potentiometer to yield 200nsec wide pulses at pin 4 of U11. This results in a write precompensation value of 200nsec.

There are four jumper options on the Floppy Disk Controller Board. They are designated on the PC Board silkscreen and are referenced on the Schematic Diagram. The jumpers should be installed as described below.

JUMPER CONNECTIONS

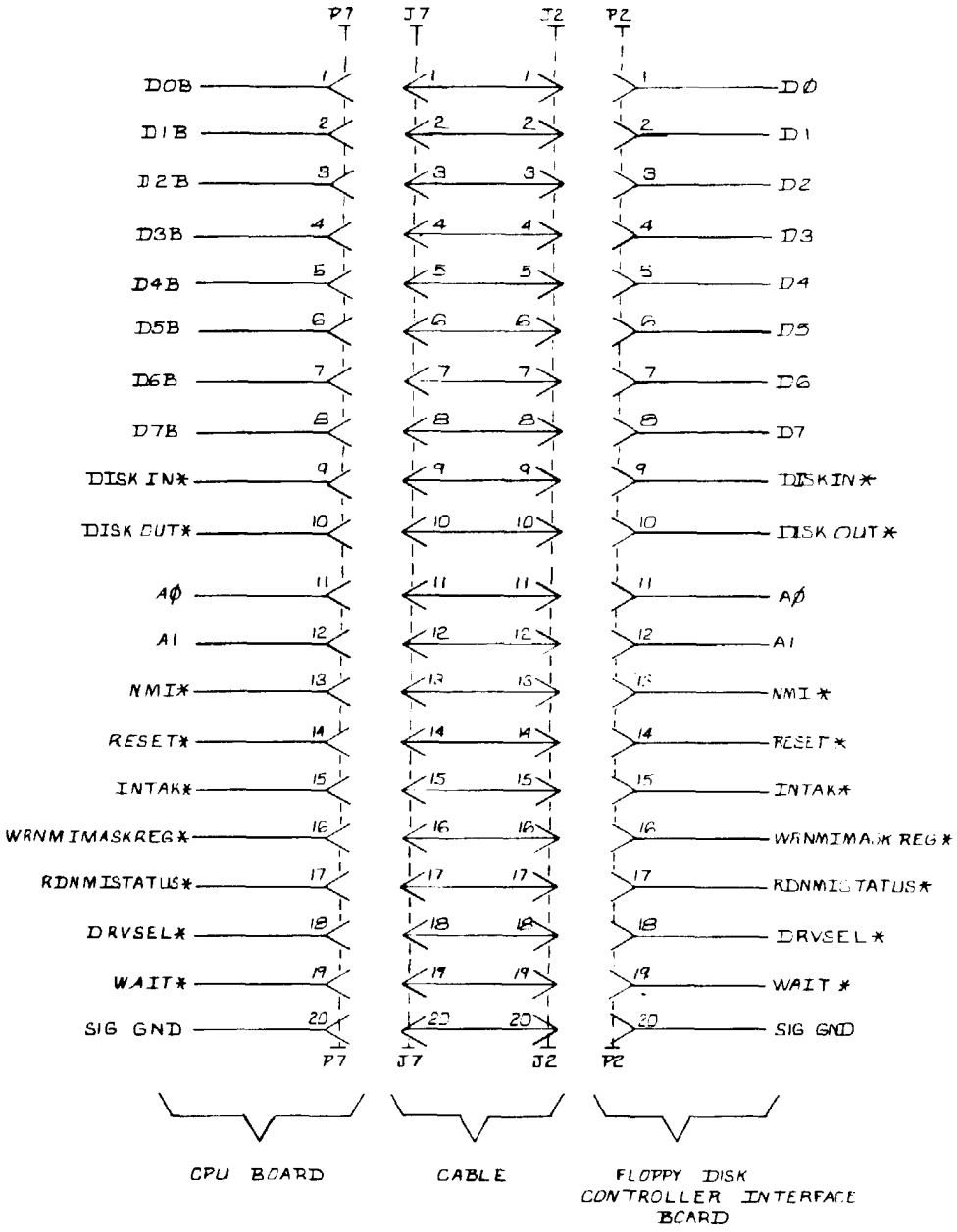
A to B

E to G

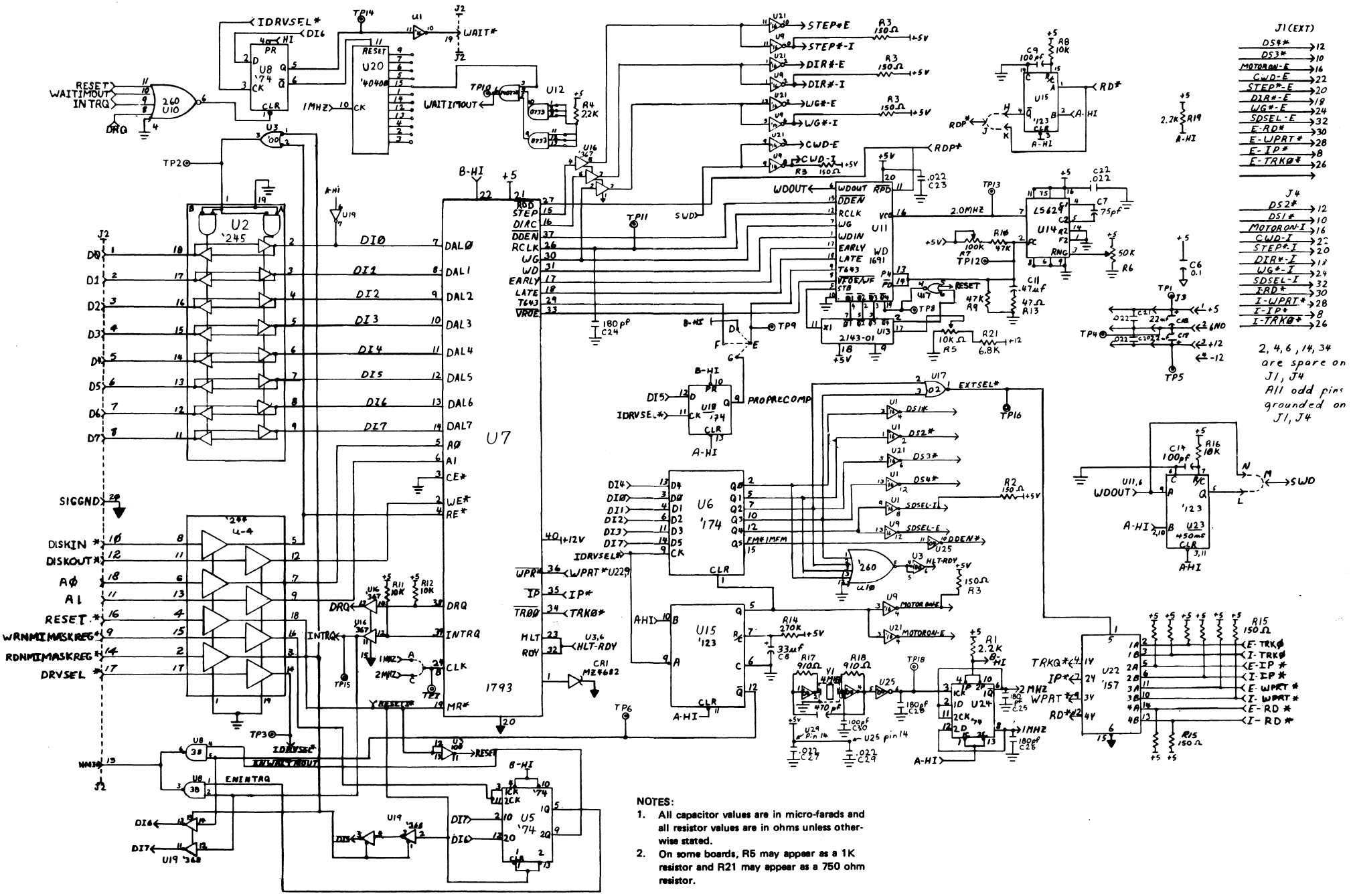
L to M

H to J

FLOPPY DISK CONTROLLER INTERFACE CONECTOR



FDC BOARD TO CPU BOARD SIGNAL DESCRIPTION



NOTES:

1. All capacitor values are in micro-farads and all resistor values are in ohms unless otherwise stated.
2. On some boards, R5 may appear as a 1K resistor and R21 may appear as a 750 ohm resistor.

SCHEMATIC 8000095E, FLOPPY DISK CONTROLLER #8858060

PARTS LIST, FLOPPY DISK INTERFACE PC BOARD #8858060

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	CAPACITORS		
C1	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C2	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C3	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C4	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C5	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C6	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C7	75pF, 50V, ceramic disc	830-0754	----------
C8	33µF, l6V, electrolytic, radial	839-6331	ACC33600AP
C9	lOOpF,50V,ceramic disc	830-1104	ACC101QJCP
C10	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C11	0.47µF, 16V, mylar	835-4471	----------
C12	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C13	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C14	lOOpF, 50V, ceramic disc	830-1104	ACC101QJCP
C15	0.lµF, 50V, monolithic, radial	838-4104	ACC104QJAP
C16	470pF, 50V, ceramic disc	830-1474	ACC47lQJCP
C17	l0µF, 16V, electrolytic, radial	832-6101	ACC106QDAP
C18	l0µF, 16V, electrolytic, radial	832-6101	ACC106QDAP
C19	0.01µF, 16V, ceramic disc	830-3104	ACC103QJCP
C20	0.022µF, 50V, ceramic disc	830-3224	ACC223QJCP
C21	0.022µF, 50V, ceramic disc	830-3224	ACC223QJCP
C22	0.022µF, 50V, ceramic disc	830-3224	ACC223QJCP
C23	0.022µF, 50V, ceramic disc	830-3224	ACC223QJCP
C24	l80pF, ceramic disc	830-1184	----------
C25	l80pF, ceramic disc	830-1184	----------
C26	l80pF, ceramic disc	830-1184	----------
C27	0.022uF, ceramic disc	830-3224	ACC223QJCP
C28	l80pF, ceramic disc	830-1184	----------
C29	0.022µF,ceramic disc	830-3224	ACC223QJCP
C30	l00pF,ceramic disc	830-1104	ACC101QJCP
	CONNECTORS		
J2	20 pos. right angle	851-9078	------
J3	4 pin right angle header	851-9079	AJ6977
	CRYSTAL		
Y1	4MHz	840-9010	AMX2804
	DIODES		
CR1	MZ4682	815-0682	A0X1518
	INTEGRATED CIRCUITS		
Ul	7416, Hex Inverter/Buffer	800-0016	-------
U2	74LS245	802-0245	AMX4470
U3	74LS00, NAND gate	802-0000	AMX3550
U4	74LS244, Octal Buffer	802-0244	AMX3864
U5	74LS74, Dual "D" Flip-Flop	802-0074	AMX3558

PARTS LIST, FLOPPY DISK INTERFACE PC BOARD

#8858060

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	INTEGRATED CIRCUITS (cont'd)		
U6	74LS174, Quad "D" Flip-Flop	802-0174	AMX3565
U7	WD1793	850-9002	AXX3041
U8	74LS38. NAND Buffer	802-0038	AMX4328
U9	7416, Hex Inverter/Buffer	800-0016	-------
Ul0	74LS260, Dual NOR gate	802-0260	-------
Ull	WD1691	850-9009	AMX4471
Ul2	MC1 40733, AND gate	803-0073	-------
U13	WD2143-01	850-9006	AMX4472
U14	74LS629, VCO	802-0629	AMX4663
U15	74LS1 23, Mono Multivibrator	802-0123	AMX3803
U16	74LS367, Hex Buffer	802-0367	AMX3567
U17	74LS02, NAND gate	802-0002	AMX3551
U18	74LS74, Dual "D" Flip-Flop	802-0074	AMX3558
U19	74LS368, Hex Inverter/Buffer	802-0368	AMX3568
U20	MC14040B, Binary Counter	803-0040	AMX4666
U21	7416, Hex Inverter/Buffer	800-0016	-------
U22	74LS1 57, Quad Multiplexer	802-0157	AMX3563
U23	74LS1 23, Mono Multiplexer	802-0123	AMX3803
U24	74LS74, Dual "D" Flip-Flop	802-0074	AMX3558
U25	74LS04, Hex Inverter	802-0004	AMX3552
	RESISTORS		
Rl	2,2K, 1/4W, 5%	820-7222	AN0216EEC
R2	150 ohm, 1/4W, 5%	820-7115	AN0142EEC
R3	150 ohm, 6 pin resistor network	829-0012	ARX024l
R4	2.2K, 1/4W, 5%	820-7222	AN0216EEC
R5	1K, Trim Pot	827-9210	AP0835
R6	50K, Trim Pot	827-9350	AP7168
R7	100K, Trim Pot	827-9410	
R8	10K, 1/4W, 5%	820-7310	AN0281EEC
R9	47K, 1/4W, 5%	820-7347	AN0340EEC
R10	47K, 1/4W, 5%	820-7347	AN0340EEC
R11	10K, l/4W, 5%	820-7310	AN0281EEC
R12	10K, l/4W, 5%	820-7310	AN0281EEC
R13	47 ohm, 1/4W, 5%	820-7047	AN0099EEC
R14	270K, 1/4W, 5%	820-7427	---------
R15	150 ohm, 10 pin resistor network	829-0013	ARX0242
R16	10K, 1/4W, 5%	820-7310	AN0281EEC
R17	910 ohm, 1/4W, 5%	820-7191	AN0192EEC
R18	910 ohm, 1/4W, 5%	820-7191	AN0192EEC
R19	2,2K, 1/4W, 5%	820-7222	AN0216EEC
R20	22K, 1/4W, 5%	820-7322	
	MISCELLANEOUS		
	Socket, 18 pin	850-9006	AJ6701
	Socket, 20 pin	850-9009	AJ6760
	Socket, 40 pin	850-9002	AJ6580
	FDC Board, complete assembly		AXX0510
	FDC Board, without major chips		AXX0509

4.2 Model 4 FDC PCB #8858160

The TRS-80 Model III/4 Floppy Disk Interface Board is an optional board which, if incorporated, provides a standard 5-1/4" floppy disk controller. The Floppy Disk Interface Board supports both single and double density encoding schemes. Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one. The amount of write precompensation provided is 250 nsec and is not adjustable. The data clock recovery logic incorporates a digital data separator which achieves state-of-the-art reliability. One to four drives may be controlled by the interface (two internal drives and two external). All data transfers are accomplished by CPU data requests. In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip. The end of the data transfer is indicated by generation of a non-maskable interrupt from the interrupt request output of the FDC chip. A hardware watchdog timer insures that any error condition will not hang the wait line to the CPU for a period long enough to destroy RAM contents.

4.2.1 Control and Data Buffering

Refer to Schematic Diagram 8000168

The Floppy Disk Controller Board is an I/O port mapped device which utilizes ports E4H, F0H, F1H, F2H, F3H, and F4H. The decoding logic is implemented on the CPU board. (Refer to Paragraph 3.1.4 Decoding Logic of the CPU operation). U4 is a non-inverting octal buffer which isolates and buffers the required control signals from the CPU board to the FDC board. U2 is a bi-directional, 8-bit trans-ceiver used to buffer data to and from the FDC board. The direction of data transfer is controlled by the combination of control signals DISKIN* and RDNMISTATUS*. If either signal is active (logic low), U2 is enabled to drive data onto the CPU board data bus. If both signals are inactive (logic high), U2 is enabled to receive data from the CPU board data bus.

4.2.2 Nonmaskable Interrupt Logic

A dual D flip-flop (U12) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMIMASKREG*. The outputs of U12 enable the conditions which will generate a non-maskable interrupt to the CPU. The NMI interrupt conditions are programmed by doing an OUT instruction to port E4H with the appropriate bits set. If data bit 7 is set, an FDC interrupt request is enabled to generate an NMI interrupt. If data bit 7 is reset, interrupt requests from the FDC are disabled. If data bit 6 is set, a Motor Time Out is enabled to generate a NMI interrupt. If data bit 6 is reset, interrupts on Motor Time Out are disabled. An IN instruction from port E4H enables the CPU to check the FDC board to determine the source of the non-maskable interrupt. Data bit 7 indicates the status of FDC interrupt request (0 = true, 1 = false). Data bit 6 indicates the status of Motor Time Out (0 true, 1 false). Data bit 5 indicates the status of the Reset signal from the CPU board (0 = true, 1 = false). The control signal RDNMISTATUS* gates this status onto the CPU data bus when active (logic low).

4.2.3 Drive Select Latch and Motor ON Logic

Selecting a drive prior to a disk I/O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set. The following table described the bit allocation of the Drive Select Latch:

Data Bit	Function
D0	Selects Drive 0 when set*
D1	Selects Drive 1 when set*
D2	Selects Drive 2 when set*
D3	Selects Drive 3 when set*
D4	Selects Side 0 when reset Selects Side 1 when set
D5	Write precompensation enabled when set, disabled when reset
D6	Generates WAIT if set
D7	Selects MFM mode if set Selects FM mode if reset

*Only one of these bits should be set per output

A hex D flip-flop (U5) latches the drive select bits, side select and FM*/MFM bits on the rising edge of the control signal IDRVSEL*. A dual D flip-flop (U15) is used to latch the Wait Enable and Write precompensation enable bits on the rising edge of IDRVSEL*. The rising edge of IDRVSEL* also triggers a one-shot (1/2 of U13) which produces a Motor On to the disk drives. The duration of the Motor On signal is approximately two seconds. The spindle motors are not designed for continuous operation, therefore the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected. The Motor On one-shot is retriggerable by simply executing another OUT instruction to the Drive Select Latch.

4.2.4 Wait State Generation and WAITIMOUT Logic

As previously mentioned, a wait state to the CPU can be initiated by an OUT to the Drive Select Latch with D6 set. Pin 5 of U1 5 will go high after this operation. This signal is inverted by 1/6 of U1 and is routed to the CPU board where it forces the Z-80 into a wait state. The Z-80 will remain in the wait state as long as WAIT* is low. Once initiated, the WAIT* will remain low until one of four conditions is satisfied. One half of U9 (a five input NOR gate) is used to

perform this function. INTQ, DRQ, RESET, and WAITIMOUT are the inputs to the NOR gate. If any one of these inputs is active (logic high), the output of the NOR gate (U9 pin 6) will go low. This output is tied to the clear input of the wait latch. When this signal goes low, it will clear the Q output (U18 pin 5) and set the Q* output (U15 pin 6). This condition causes WAIT* to go high which allows the Z-80 to exit the wait state. U3 is a 12-bit binary counter which serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents. The counter is clocked by a 1 MHz clock and is enabled to count when its reset pin is low (U3 pin 11). A logic high on U3 pin 11 resets the counter outputs. U3 pin 15 is a divide-by-1024 output and is used to generate the signal WAITIMOUT. This watchdog timer logic will limit the duration of a wait to 1024 µsec, even if the FDC chip should fail to generate a DRQ or a INTRO.

4.2.5 Clock Generation Logic

A 4 MHz crystal oscillator and a 4-bit binary counter are used to generate the clock signals required by the FDC board. The 4 MHz oscillator is implemented with two inverters (1/3 of U22) and a quartz crystal (Y1). The output of the oscillator is inverted and buffered by 1/6 of U22 to generate a TTL level square wave signal. U21 is a 4-bit binary counter which is divided into a divide-by-2 and a divide-by-8 section. The divide-by-2 section is used to generate the 2MHz output at pin 12. The 2 MHz is NANDED with a MHz by 1/4 of U17 and the output is used to clock the divide-by-8 section of U21. A 1 MHz clock is generated at pin 9 of U21 which is 90 degrees phase-shifted from the 2 MHz clock. This phase relationship is used to gate the guaranty Write Data Pulse (WD) to the Write precompensation circuit. The 4 MHz is used to clock the digital data separator U11 and the Write precompensation shift register U10. The 1 MHz clock is used to drive the clock input of the FDG chip (U6) and the clock input of the watchdog timer (U3).

4.2.6 Disk Bus Selector Logic

As mentioned previously, the Floppy Disk Controller board supports up to four drives (two internal and two external). This function is implemented by using two disk drive interface buses, one for the internal drives and one for the external drives. J1 is the edge connector used to drive the internal disk drives and J4 is the edge connector used to drive the external drives. U19 (a quad 2 to 1 data selector) is used to select which set of inputs is routed from the disk drive buses to the FDC chip. U19 pin 1 is the control pin for the data selector. If pin 1 is low, the external inputs are selected, otherwise the internal inputs are selected. This control signal EXTSEL* is generated from the outputs of the Drive Select Latch. If Drive 2 or 3 is selected, U20 pin 1 will go low indicating that an external drive is selected. One half of U9 (a five-input NOR gate) is used to detect when any of the four drives is selected.

The output of the NOR gate (U9 pin 5) is inverted and is used as the head load timing (HLT) and ready (RDY) signal for the FDC chip. Therefore, if any drive is selected, the head is assumed to be loaded and the selected drive is assumed to be ready.

4.2.7 Disk Bus Output Drivers

High current open collector drivers (U18, U8, and U1) are used to buffer the output signals from the FDC board to the disk drives. Note from the schematic that each output signal to the drives has two buffers associated with each signal. One set is used for the internal drive bus and the other set is used for the external drive bus. No select logic is required for these output signals since the drive select bits define which drive is active.

4.2.8 Write Precompensation and Write Data Pulse Shaping Logic

The Write Precompensation logic is comprised of U10 (74LS195), 1/4 of U17, 1/4 of U20, and 1/2 of U15. U10 is a parallel in, serial out shift register and is clocked by 4 MHz which generates a precompensation value of 250 nsec. The output signals EARLY and LATE of the FDC chip (U6) are input to P0 and P2 of the shift register. A third signal is generated by 1/4 of U20 when neither EARLY nor LATE is active low and is input to P1 of U10. WD of the FDC chip is NANDed with 2 MHz to gate the guaranteed Write Data Pulse to U10 for the parallel load signal SHFT/LD. When U10 pin 9 is active low, the signals preset at P1-P3 are clocked in on the rising edge of the 4 MHz clock. After U10 pin 9 goes high, the data is shifted out at a 250 nsec rate. EARLY will generate a 250 nsec delay, NOT EARLY AND NOT LATE will generate a 500 nsec delay, and LATE will generate a 750 nsec delay. This provides the necessary precompensation for the write data. As mentioned previously, Write Precompensation is enabled through software by an OUT to the Drive Select Latch with bit 5 set. This sets the Q output of the 74LS74 (U15 pin 9) which disables the shift register U10. This signal also enables U20 to allow the write data (WD) to bypass the Write Precompensation circuit. The Write Date (WD) pulse is shaped by a one-shot (1/2 of U3) which stretches the data pulses to approximately 500 nsec.

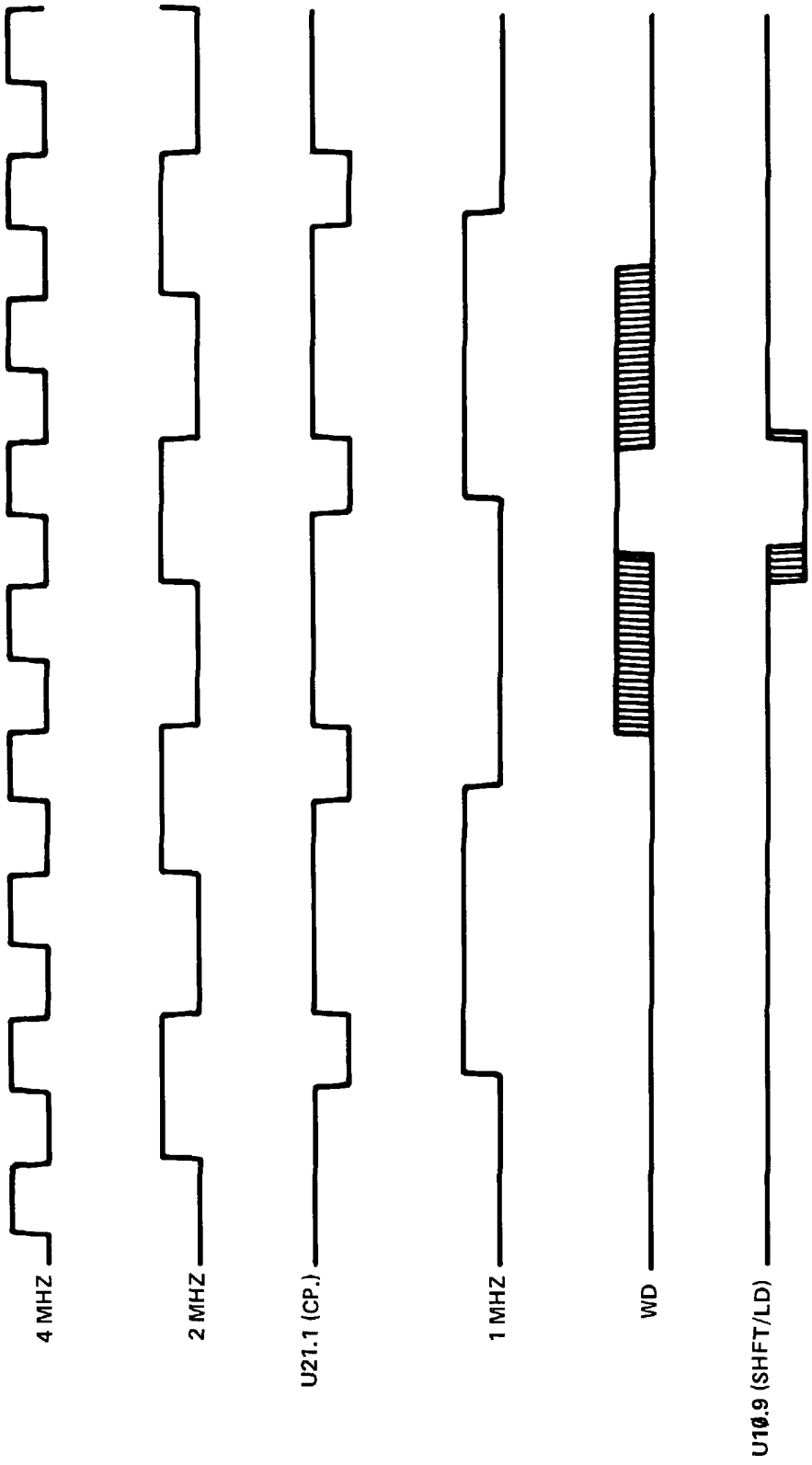


FIGURE 4-1. WRITE PRECOMPENSATION TIMING

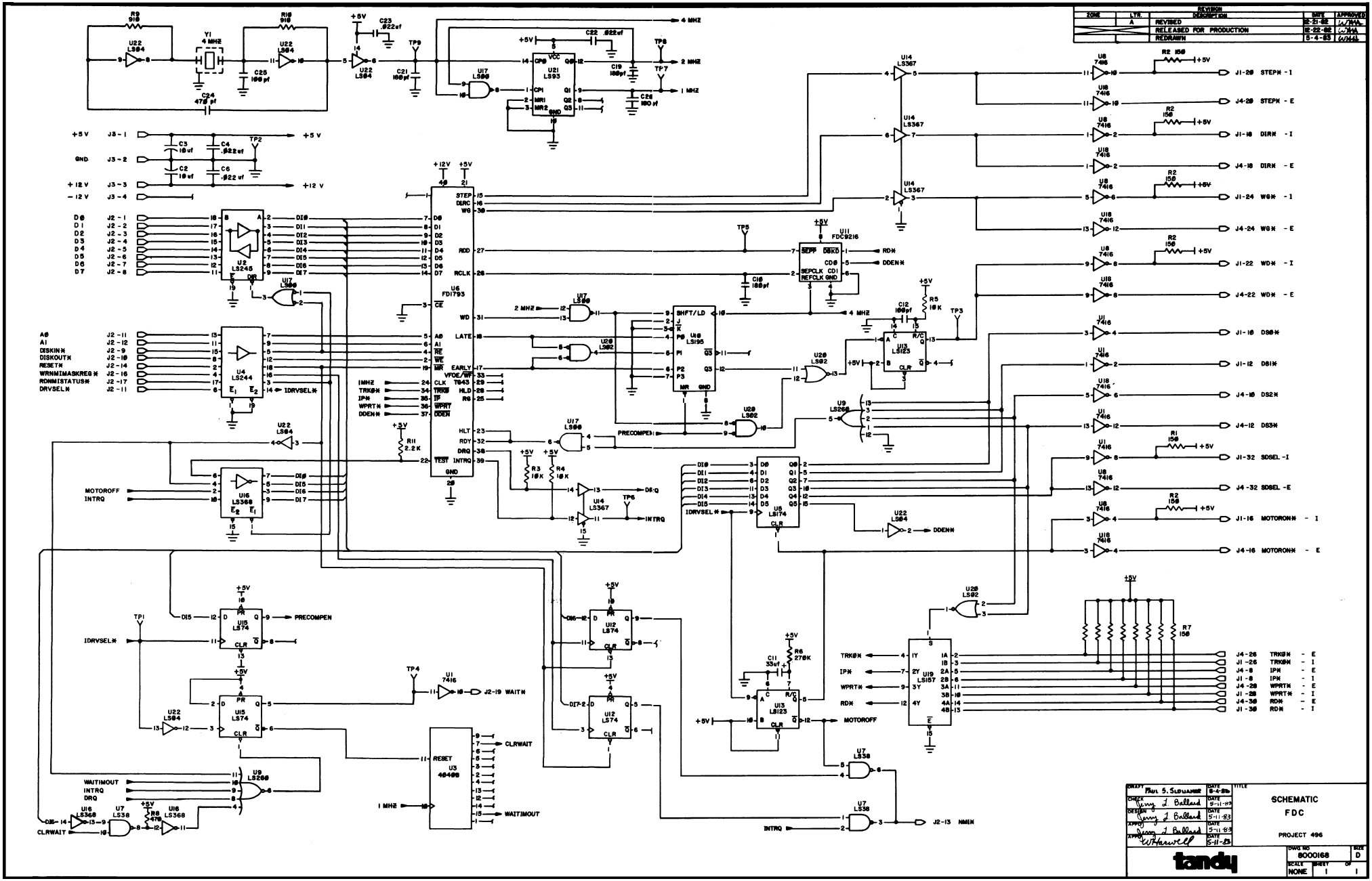
4.2.9 Clock and Read Data Recovery Logic

The Clock and Read Data Recovery Logic is comprised of one chip, the FDC9216. The FDC9216 is a Floppy Disk Data Separator (FDDS) which converts a single stream of pulses from the disk drive into separate clock and data pulses for input to the FDC chip. The FDDS consists of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. The reference clock (REFGLK) is 4 MHz and is divided by the internal clock divider. CD0 and CD1 of the FDDS chip control the divisor which divides REFCLK. With CD1 grounded (logic low), CD0 (when a logic low) generates a divide-by-1 for MFM mode and when logic high generates a divide-by-2 for FM mode. CD0 is controlled by the signal DDEN* which is Double Density Enable or MFM enable. The FDDS detects the leading edges of RD* pulses and adjusts the phase of the internal clock to generate the separated clock (SEPCLK) to the FDC chip. The separate long and short term timing correctors assure the clock separation to be accurate. The separated Data (SEPD*) is used as the RDD* input to the FDC chip.

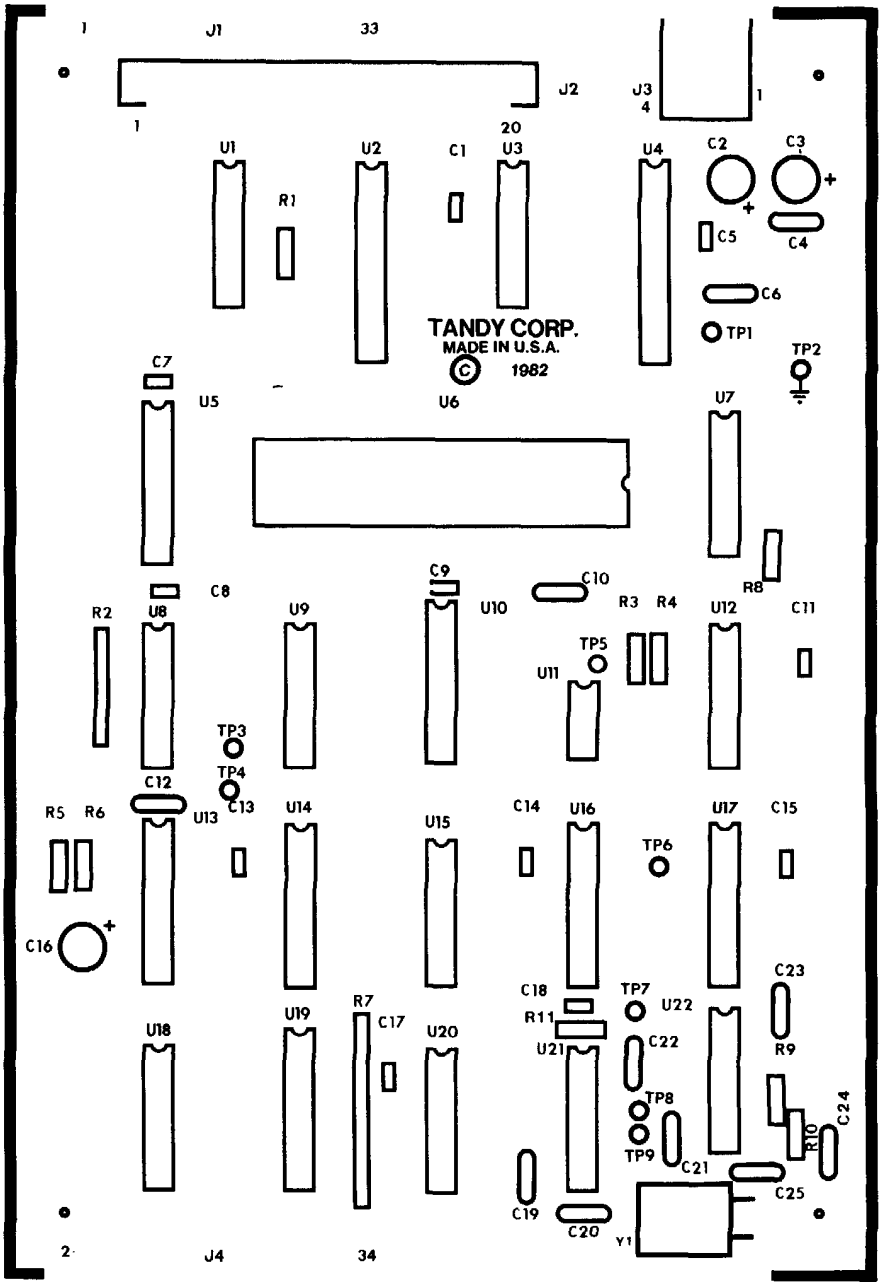
4.2.10 Floppy Disk Controller Chip

The 1793 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation. The 1793 is functionally identical to the 1791 used on the Model II FDC Printer Interface Board except that the data bus is true as opposed to inverted. Refer to the appendix section for more information on the FD1793. The Model II Technical Reference Manual also contains a good presentation of the 1791 FDC chip as well as a discussion on Write precompensation. The following port addresses are assigned to the internal registers of the 1793 FDC chip:

Port #	Function
F0H	Command/Status Register
F1H	Track Register
F2H	Sector Register
F3H	Data Register



SCHEMATIC 8000268, FDC PCB #8858160



COMPONENT LAYOUT #1700223C, FLOPPY DISK CONTROLLER PCB #8858160

Parts List, FDC PCB #8858160

Item	Qty	Description	Mfgr's Part No.
1	1	Printed Circuit Board	8709380
2	9	staking Pin (TP1-9)	8529014
3	1	Connector, 20-Pin Rt. Angle (J2)	8519078
4	1	Connector, 4-Pin Rt. Angle (J3)	8519079
5	1	Socket, 8-Pin (Ull)	8509011
6	1	Socket, 40-Pin (U6)	8509002
7	1	Resistor, 150 ohm 1/4w 5% (R1)	8207115
8	1	Resistor Pak, 150 ohm 6-Pin (R2)	8290012
9	3	Resistor, 10K ohm 1/4w 5% (R3-5)	8207310
10	1	Resistor, 270K ohm 1/4w 5% (R6)	8207427
11	1	Resistor Pak, 150 ohm 10-Pin (R7)	8290013
12	1	Resistor, 470 ohm 1/4w 5% (R8)	8207147
13	2	Resistor, 910 ohm 1/4w 5% (R9,10)	8207191
14	1	Resistor, 2.2K ohm 1/4w 5% (R11)	8297222
15	11	Capacitor, 0.1 ufd 50V (C1,5,7-9,11,13-15,C17,18)	8374104
16	2	Capacitor, 10 ufd 16V Elec. (C2,3)	8326101
17	4	Capacitor, .022 ufd 50V (C4,6,22,23)	8303224
18	4	Capacitor, 180 pfd 50V C. Disk (Cl0,19-21)	8301184
19	2	Capacitor, 100 pfd 50V C. Disk (C12,25)	8301104
20	1	Capacitor, 33 ufd 16V Elec. (C16)	8396331
21	1	Capacitor, 470 pfd 50V C. Disk (C24)	8301474
22	1	Crystal, 4.000 MHz (Y1)	8409010
23	3	IC, 7416 Hex Inverter Buffer (U1,8,18)	8000016
24	1	IC, 74LS245 Octal Bus Tranceiver (U2)	8020245
25	1	IC, MC14040 Binary Counter (U3)	8030040
26	1	IC, 74LS244 Octal Buffer (U4)	8020244
27	1	IC, 74LS174 Flip Flop (U5)	8020174
28	1	IC, 1793 FDC (U6)	8030793
29	1	IC, 74LS38 NAND Buffer (U7)	8020038
30	1	IC, 74LS260 5-In NOR Gate (U9)	8020260
31	1	IC, 74LS195 Shift Register (Ul0)	8020195
32	1	IC, 9216 Data Separator (Ull)	8040216
33	2	IC, 74LS74 Flip Flop (U12,15)	8020074
34	1	IC, 74LS123 Mono Multiplier (U13)	8020123
35	1	IC, 74LS367 Hex Buffer (U14)	8020367
36	1	IC, 74LS368 Hex Inv. Buffer (U16)	8020368
37	1	IC, 74LS00 NAND Gate (U17)	8020000
38	1	IC, 74LS157 Quad Multiplier (U19)	8020157
39	1	IC, 74LS02 NOR Gate (U20)	8020002
40	1	IC, 74LS93 4-Bit Counter (U21)	8020093
41	1	IC, 74LS04 Hex Inverter (U22)	8020004

SECTION V

MINI-DISK DRIVE

SECTION VI

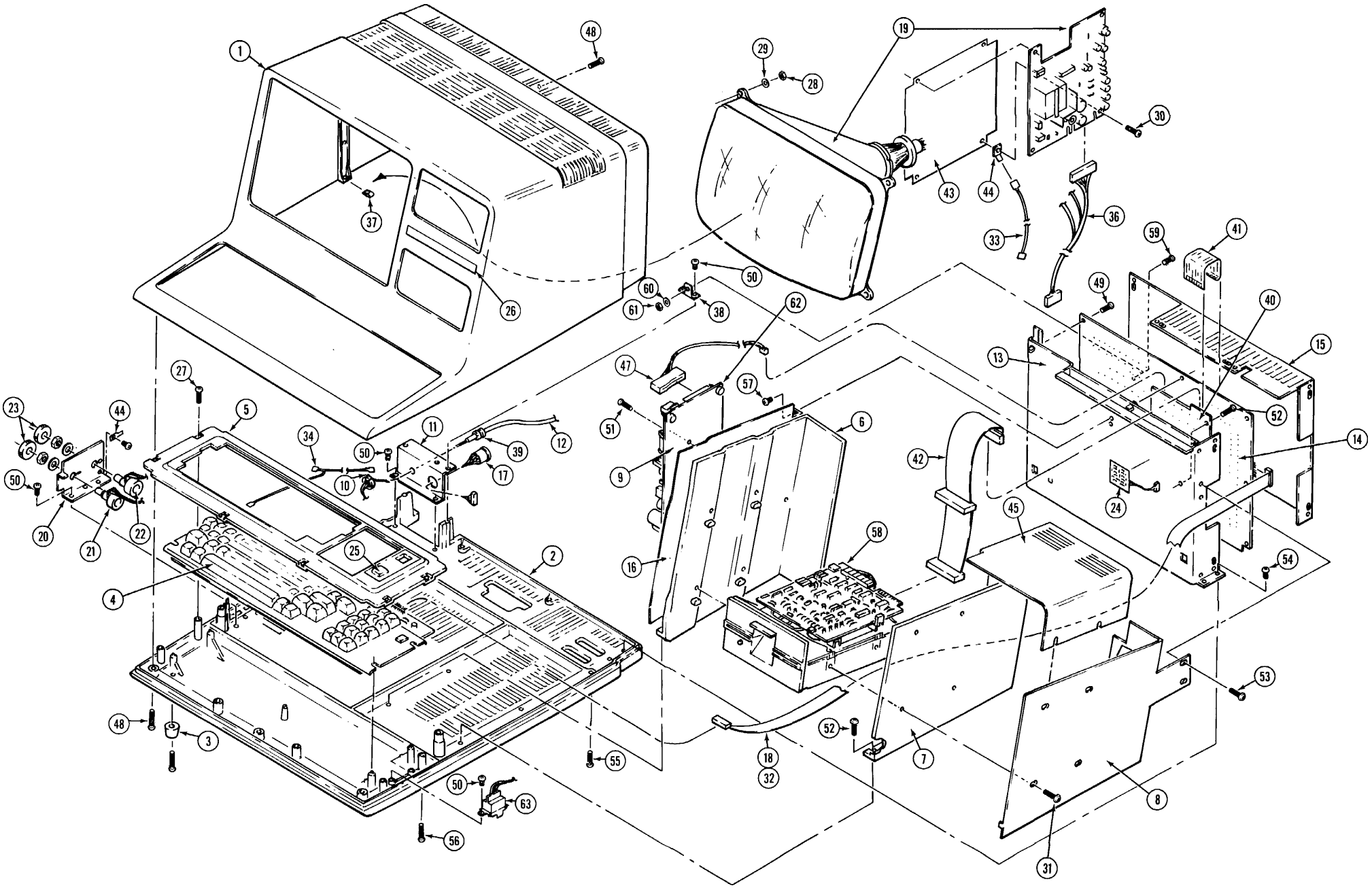
POWER SUPPLIES

SECTION VII

VIDEO MONITOR

SECTION VIII

ILLUSTRATED PARTS CATALOG



EXPLODED VIEW, MODEL 4 COMPUTER, CATALOG #26-1067/8/9

Parts List, Model 4 Computer, #26-1067/8/9

Item	Qty	Description	Mfgr's PN	RS Part No
1	1	Case Top	8719104	
2	1	Base	8719265	
3	4	Feet, Case	8590098	
4	1	Keyboard	8790524	
5	1	Keyboard Bezel	8719164	
6*	1	Bracket, Disk Mounting (LH)	8719106	
7*	1	Bracket, Disk Mounting (RH)	8719105	
8*	1	Shield, Disk (RH side)	8729093	
9	1	Power Supply Assy.(on 26-1067)	8790021	AXX5019
		(on 26-1068/1069)	8790043 or 8790049	
10	1	Toroid	8419030	
11	1	Bracket, Connector	8729039	ART3082
12	1	Cord, Power	8709412	
13	1	Chassis	8858073	
14	1	Main Logic PCB Assembly	6700104	
		(on 26-1067)		
		(on 26-1068/1069)	8858090	
15	1	Shield, Chassis	8729049	
16*	1	Shield, Disk (LH side)	8729041	
17	1	Cable Assembly, Cassette	8709372	
18	1	Cable, Flat	8709381	
19	1	Video Display, CRT (RCA)	8492002	AXX80L0
		Video Display, CRT (TCE)	8790607	
20	1	Bracket, Pot Mounting	8729155	
21	1	Pot, 500 ohms (Contrast)	-------	
		(part of Item 36)		
22	1	Pot, 500K ohms (Brightness)	-------	
		(part of Item 36)		
23	2	Knob, Thumbwheel	8719112	AK4298
24*	1	Sound PCB Assembly (26-1068/1069 only)	8858121	
25	1	Label, RAM size (16K)	8789261	AHC0321
		(64K)	8789800	
26	1	Name Plate	8719266	
27	6	Screw, #6 x 3/8″	8569047	
28	4	Nut, #10-24 Hex	8579021	
29	4	Washer, #8 Flat	8589016	
30	2	Screw, #6 x 3/8″	8569047	
31	8	Screw, #6-32 x 1/2″	8569046	
32	1	Cable, Keyboard Ground	8709275	

Parts List, Model 4 Computer, #26-1067/8/9
* Not used on Model #26-1067

Parts List, Model 4 Computer, #26-1067/8/9

Item	Qty	Description	Mfgr's PN	RS Part No
33	1	Cable, Ground	8709193	
34	1	Ground, Main	8709161	
35	1	Clip, Tinnerman	8559031	
36	1	Cable Assembly, CRT	8709369	
		for Models 26-1068/1069		
		for Model 26-1067	8709286	
37	5	Clip, Tinnerman	-------	
38	1	Bracket, Support	8729055	
39	1	Strain Relief, Power Cord	8559014	
40*	1	FDC PCB Assembly	8858060 or 8858160	
41*	1	Flat Cable Assembly	8459020	
42*	1	Cable Assembly, Disk Drive	8709154	
43	1	Shield, CRT PCB Assembly	8539014	
44	2	Tab, Grounding	8529020	
45	1	Shield, Disk Drive Top (used on 26-1069 only)	8729175	
46	1	Shield, Mylar	8539015	
47	1	Cable Assembly, DC Power	8709367	
		for 26-1068/9		
		for 26-1067	8709178	
48	3	Screw, #8-32 x 3/4″ PPH Blk	8569047	
49	8	Screw, #6-32 x 1/2″ PPH	8569046	
50	4	Screw, #6 x 1/4″ Plastite	8569077	
51	6	Screw, #8-32 x 1/2″	8569140	
52	4	Screw, #6-32 x 1/4″	8569098	
53*	12	Screw, #6 x 3/8″ Washer	8569128	
54	4	Screw, Chassis Mounting	8569077	
55	5	Screw, #8 x 1″	8569095	
56	2	Screw, #8-32 x 1″	8569084	
57	2	Screw, #6 x 3/8″	8569047	
58*	2**	Disk Drive Assembly	8790112	
59	2	Screw, #6-32 x 1/4″	8569098	
60	1	Washer, #6 Internal Star	8589043	
61	2	Nut, #6 Hex	8579014	
62*	3	Standoff, Power Supply	8589079	
63	1	Switch, DPST (ON-OFF)	8489030	

* Not Used On 26-1067 Computer
** Qty Of 1 On 26-1068 Computer

SECTION IX

RS-232C CIRCUIT BOARD

RS-232C CIRCUIT BOARD

9.1 RS-232C Technical Description

The RS-232C option board for the Model 4 computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input - output interface (P1). The heart of the board is the TR1602 Asynchronous Receiver/Transmitter. It performs the job of converting the parallel byte date from the CPU to a serial data stream including start, stop, and parity bits. For a more detailed description of how this LSI circuit performs these functions, refer to the TR1602 data sheets and application notes. The transmit and receive clock rates that the TR1602 needs are supplied by the Baud rate generator (BR19411). This circuit takes the 5.0688 MHz supplied by the CPU board and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks. The rates available from the BRG go from 50 Baud to 19200 Baud. See the BRG table for the complete list.

BRG PROGRAMMING TABLE

NIBBLE LOADED	TRANSMIT OR RECEIVE BAUD RATE	16X CLOCK FREQUENCY	SUPPORTED BY SETCOM
0H	50	0.8kHz	yes
1H	75	1.2 kHz	yes
2H	110	1.76kHz	yes
3H	134.5	2.1523kHz	yes
4H	150	2.4kHz	yes
5H	300	4.8kHz	yes
6H	600	9.6 kHz	yes
7H	1200	19.2 kHz	yes
8H	1800	28.8kHz	yes
9H	2000	32.081 kHz	yes
AH	2400	38.4 kHz	yes
BH	3600	57.6kHz	yes
CH	4800	76.8 kHz	yes
DH	7200	115.2kHz	yes
EH	9600	153.6kHz	yes
FH	19,200	307.2kHz	yes

The RS-232C board is a port mapped device and the ports used are E8 to EB. Following is a description of each port on both input and output.

PORT	INPUT	OUTPUT
E8	Modem status	Master Reset, enables UART control register load
EA	UART status	UART control register load and modem control
E9	Not Used	Baud rate register load enable bit
EB	Receiver Holding register	Transmitter Holding register

Interrupts are supported on the RS-232C option board by the Interrupt mask register (U10) and the Status register (U9) which allows the CPU to see which kind of interrupt has occurred. Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors - parity, framing, or data overun. This allows a minimum of CPU overhead in transferring data to or from the UART. The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read). Refer to the IO Port description for a full breakdown of all interrupts and their bit positions.

The Model 4 RS-232C board is functionally identical to the Model I RS-232 board with the following exceptions:

Interrupts are supported, there are no sense switches for configuring the interface, there is no COM/TERM switch for reversing the function of pins 2 and 3 on the DB-25. and the DC to DC converter is not required since +12V and -12V are provided by the internal power supply. Other differences include three additional interface outputs and no crystal for the BRG. All Model I software written for the RS-232 interface is compatible with the Model 4 RS-232C option board, provided that the software does not use the sense switches to configure the interface. The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface. The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145).

9.2 Pinout Listing

The following list is a pinout description of the DB-25 connector (P1).

PIN#	SIGNAL
1	PGND (Protective Ground)
2	TD (Transmit Data)
3	RD (Receive Data)
4	RTS (Request To Send)
5	CTS (Clear To Send)
6	DSR (Data Set Ready)
7	SGND (Signal Ground)
8	CD (Carrier Detect)
20	DTR (Data Terminal Ready)
22	RI (Ring Indicate

9.3 Port and Bit Assignments

PORT E8H
OUTPUT: MASTER RESET
INPUT: MODEM STATUS REGISTER

An output to this port (and data), performs a master reset to the UART and enables the control register load enable bit. The following table details the bit definitions for an input from port E8H.

DATA BIT	FUNCTION
D7	Clear To Send, Pin 5 DB-25
D6	Data Set Ready, Pin 6 DB-25
D5	Carrier Detect, Pin 8 DB-25
D4	Ring Indicator, Pin 22 DB-25
D3	Not Used
D2	Not Used
D1	Not Used
D0	Receiver Input, UART Pin 20 DB-25

PORT E9H
OUTPUT: BAUD RATE LOAD
INPUT: NOT USED

An output to this port loads the Baud rate generator with a code which corresponds to the desired receive and transmit Baud rate as outlined in the BRG Programming Table. The low order nibble of the data output to this port determines the receiver Baud rate, while the high order nibble determines the transmit Baud rate.

PORT EAH
OUTPUT: UART AND MODEM CONTROL
INPUT: UART STATUS

An output to this port loads the UART Control register if the enable bit for this function is set (D1 port E8H = 1). The UART Control register is five bits wide (D7 - D3) leaving three bits for modem control (D2 - D0). Three more modem control bits were added by allowing software to enable or disable the UART Control register. The tables below summarize the bit allocations with the UART Control register enabled and disabled.

PORT EAH OUTPUT BITS WITH UART CONTROL REGISTER ENABLED

DATA BIT	FUNCTION
D7	Even Parity Enable, 1 = even, 0 = odd
D6	Word Length Select 1
D5	Word Length Select 2
D4	Stop Bit Select, 1 two stop bits, 0 = one stop bit
D3	Parity Inhibit, 1 = disable parity
D2	Break 0 = disable transmit data (continuous space)
D1	Data Terminal Ready, Pin 20 DB-25
D0	Request To Send, Pin 4 DB-25

PORT EAH OUTPUT BITS WITH UART CONTROL REGISTER DISABLED

DATA BIT	FUNCTION
D7	Not Used
D6	Not Used
D5	Secondary unassigned, Pin 18 DB-25
D4	Secondary Transmit Data, Pin 14 DB-25
D3	Secondary Request To Send, Pin 19 DB-25
D2	Break 0 = disable Transmit Data (continuous space)
D1	Data Terminal Ready, Pin 20 DB-25
D0	Request To Send, Pin 4 DB-25

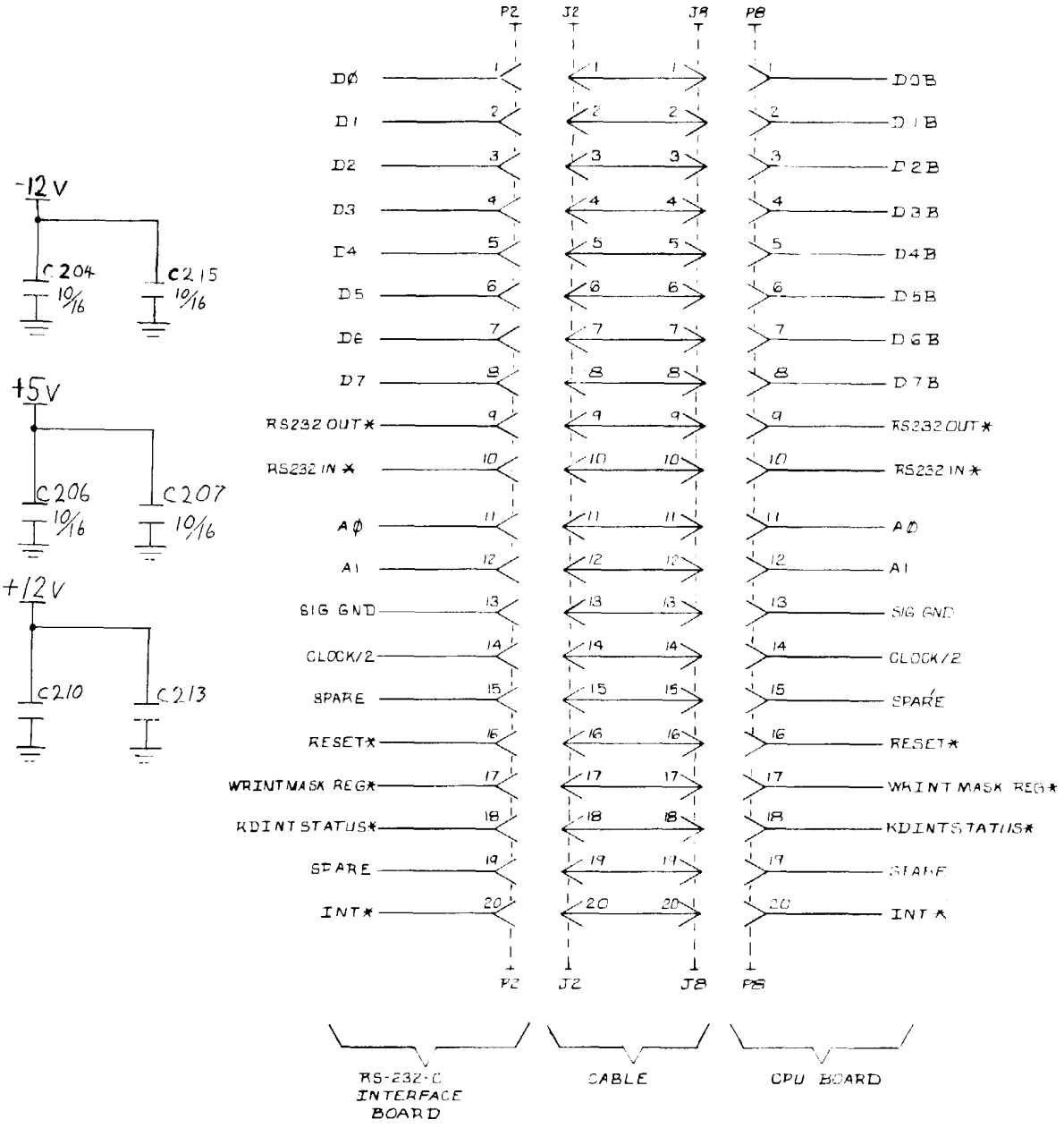
PORT EAH INPUT BITS

DATA BITS	FUNCTION
D7	Data Received, 1 = condition true
D6	Transmitter Holding register empty, 1 = condition true
D5	Overrun error, 1 = condition true
D4	Framing error, 1 = condition true
D3	Parity error, 1 = condition true
D2	Not Used
D1	Not Used
D0	Not Used

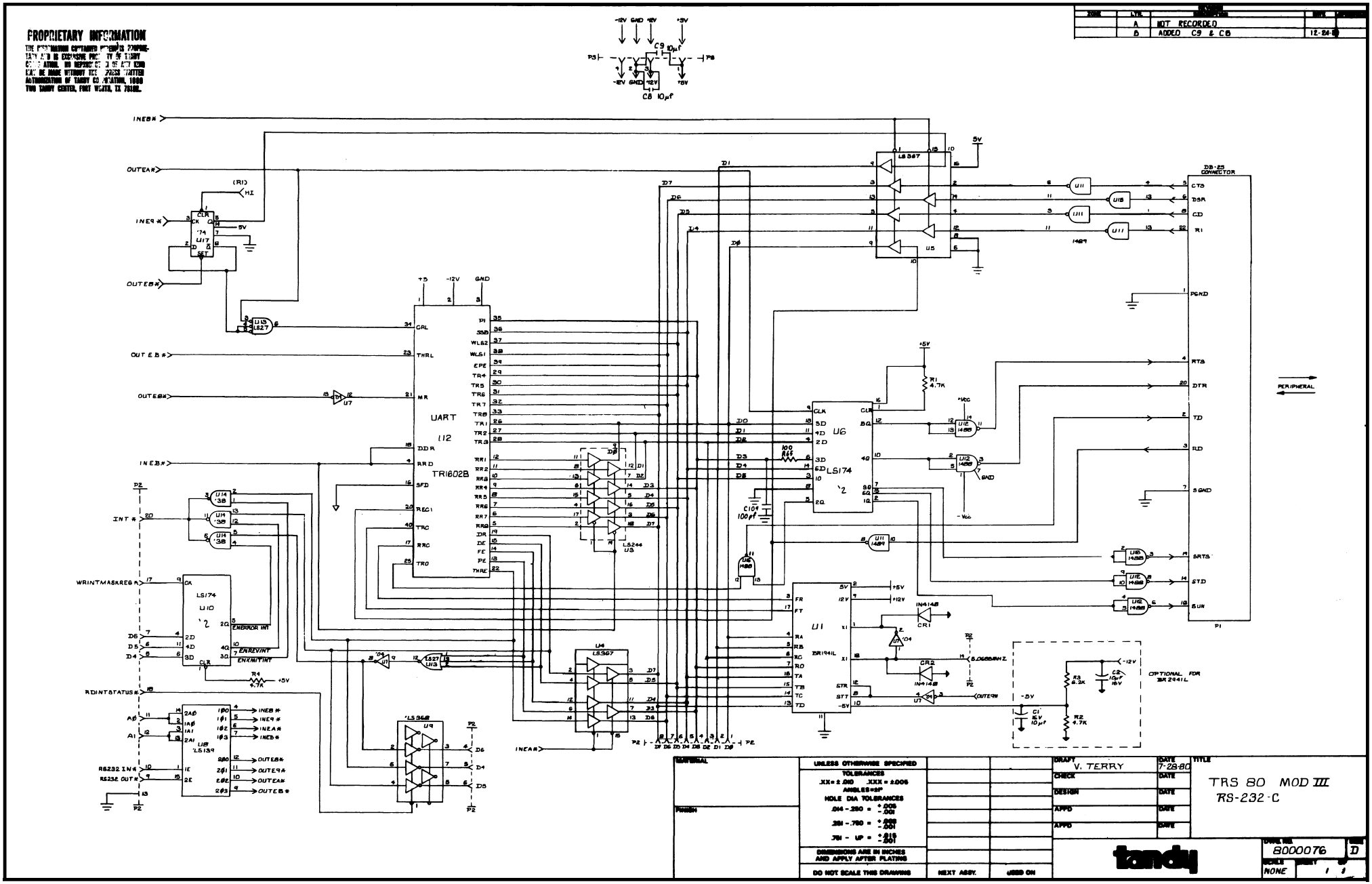
PORT EBH
OUTPUT: TRANSMITTER HOLDING REGISTER
INPUT: RECEIVER HOLDING REGISTER

An output to this port loads the UART Transmitter Holding register with a word to be transmitted, as soon as the last word loaded in the holding register is transmitted. This register should never be loaded until the Transmitter Holding register empty bit (port EAH) is true. An input from this port reads the last word received from the UART received data holding register. This register should not be read until the data received bit (port EAH) is true.

RS-232-C INTERFACE CONNECTOR



RS-232 BOARD TO CPU BOARD SIGNAL DESCRIPTION


PROPRIETARY INFORMATION
TRS 80 MOD III
RS-232-C
8000076
UART
TR1602B
LS174
LS367
LS368
LS244
1489
1488
1489A
1488
1488
1488

PARTS LIST RS-232C PC BOARD

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	CAPACITORS		
C1	l0µF, 16V, radial (optional)	832-6101	ACC106QDAP
C2	l0µF, 16V, radial (optional)	832-6101	ACC106QDAP
C3	0.1µF, 50V, monolithic, radial	838-4104	ACC104QJAP
C4	0.1µF, 50V, monolithic, radial	838-4104	ACC104QJAP
C5	0.1µF, 50V, monolithic, radial	838-4104	ACC104QJAP
C6	0.1µF, 50V, monolithic, radial	838-4104	ACC104QJAP
C7	0.1µF, 50V, monolithic, radial	838-4104	ACC104QJAP
C8	l0µF, 16V, radial	832-6101	ACC106QDAP
C9	l0µF, 16V, radial	832-6101	ACC106QDAP
	CONNECTORS		
P1	DB-25 Connector	851-9030	------
P2	20 pos. right angle	851-9078	------
P3	4 pos. right angle	851-9079	AJ6977
	INTEGRATED CIRCUITS		
Ul	8R1941-L,Dual Baud C	804-6941	AMX3921
U2	TR1602B, UART	804-5602	AMX3865
U3	74LS244, Octal Buffer	802-0244	AMX3864
U4	74LS367, Hex Buffer	802-0367	AMX3567
U5	74LS367, Hex Buffer	802-0367	AMX3567
U6	74LS174, Quad "D" Flip-Flop	802-0174	AMX3565
U7	7404, Hex Inverter		AMX3655
U8	74LS139, Dual Decoder	802-0139	AMX3800
U9	74LS368, Hex Buffer	802-0368	AMX3568
U10	74LS174, Quad "D" Flip-Flop	802-0174	AMX3565
U11	MC1489, Quad Line Driver	805-0189	AMX3868
U12	MC1488,Quad Line Driver	805-0188	AMX3867
U13	74LS27,NOR gate	802-0027	-------
U14	74LS38, NAND Buffer	802-0038	AMX4328
U15	MC1489, Quad Line Driver	805-0189	AMX3868
U16	MC1488,Quad Line Driver	805-0188	AMX3867
	RESISTORS		
R1	4.7K, 1/4W, 5%	820-7247	AN0247EEC
R2	4.7K, 1/4W, 5% (optional)	820-7247	AN0247EEC
R3	6.2K, 1/4W, 5% (optional)	--------	AMX4658
R4	4.7K, 1/4W, 5%	820-7247	AN0247EEC
	MISCELLANEOUS		
	Cable, 20 pos., 4.5", flat	845-9020	AW2631
	Socket, 18 pin	850-9006	AJ6701
	Socket, 40 pin	850-9002	AJ6580